Program Highlights		
19th August 2012 (Sunday)		
1:30PM--2:00PM	Delegate Arrival and Registration	
2:00PM--3:00PM	**Session -- 01 (Ph. D. Forum)**	
3:00PM--4:30PM	**Session – 02 (SS--Projects)**	**ISVLSI Committee Meeting**
20th August 2012 (Monday)		
8:00AM -- 8:30AM	Registration, Breakfast	
8:30AM -- 8:45AM	**Inaugural Event**	
8:45AM -- 9:45AM	**Keynote Address**	
9:45AM -- 10:00AM	Break	
10:00AM -- 11:00AM	**Session – 03 (NoC)**	**Session – 04 (Thermal)**
11:00AM -- 12:30PM	**Session – 05 (SS--Cypto-Architecture)**	**Session – 06 (SS--RRAM)**
12:30PM -- 2:00PM	Lunch	
2:00PM -- 3:00PM	**Session – 07 (Logic-Synthesis)**	**Session – 08 (Advanced-Circuit)**
3:00PM -- 4:00PM	**Session – 09 (Emerging-Technology)**	**Session – 10 (Hardware-Security)**
4:00PM -- 4:15PM	Tea break	
4:15PM -- 5:00PM	**Plenary Talk -- 1**	
5:00PM -- 6:00PM	**Session – 11 (Reliability)**	**Session – 12 (Reversible-Design)**
6:00PM – 6:30PM	Break	
6:30PM -- 8:30PM	**Symposium Banquet**	
21st August 2012 (Tuesday)		
8:00AM -- 8:30AM	Registration, Breakfast	
8:30AM -- 9:15AM	**Plenary Talk -- 2**	
9:15AM -- 10:15AM	**Session – 13 (Datapath-Design)**	**Session – 14 (Design-Archictrure)**
10:15AM -- 11:15AM	**Session – 15 (Analog-Design)**	**Session – 16 (SS--Parser)**
11:15AM – 12:15PM	**Session – 17 (Design-Fabric)**	**Session – 18 (Design-Modeling)**
12:15PM -- 1:45PM	Lunch	
1:45PM -- 2:30PM	**Plenary Talk -- 3**	
2:30PM -- 4:00PM	**Session – 19 (SS--Secure-Systems)**	**Session – 20 (SS--EMT)**
4:00PM -- 5:30PM	**Session -- 21 (SS--NVM)**	
5:30PM -- 5:45PM	**ISVLSI 2012 Closing Remarks**	

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Program Schedule

19th August 2012 (Sunday)

1:30PM--2:00PM	Delegate Arrival and Registration	
2:00PM--3:00PM	**Session -- 01** **Session Title: Ph. D. Forum** **Session Chair:** Michael Hübner, michael.huebner@ruhr-uni-bochum.de, Karlsruhe Institute of Technology, Germany **Papers:** Youngsoo Kim, William W Edmonson and Winser E Alexander: **A Dataflow Framework for DSP Algorithm Refinement** Daniel Limbrick: **Impact of Logic Synthesis on Soft Error Rate of Digital Integrated Circuits** Himanshu Thapliyal and Nagarajan Ranganathan: **Design, Synthesis and Test of Reversible Circuits for Emerging Nanotechnologies** Sudip Roy, Partha P. Chakrabarti, and Bhargab B. Bhattacharya: **Algorithms for On-Chip Solution Preparation using Digital Microfluidic Biochips**	
3:00PM--4:30PM	**Session – 02** **Session Title**: Projects **Session Chair**: Juergen Becker, juergen.becker@kit.edu, Karlsruhe Institute of Technology Jürgen Becker: **Architecture oriented paraLlelization for high performance embedded Multicore systems using scilAb** Gabriel Marchesan Almeida: **FlexTiles: A self-adaptive heterogeneous many-core architecture based on flexible tiles** Zlatko Petrov: **Rendering FPGAs to Multi-Core Embedded Computing**	**ISVLSI Committee Meeting**

20th August 2012 (Monday)

8:00AM -- 8:30AM	Registration, Breakfast

8:30AM -- 8:45AM	**Inaugural Event**	
8:45AM -- 9:45AM	**Keynote Address** Andrew Kahng, abk@cs.ucsd.edu, The University of California San Diego, Title: DfX and Signoff: The Coming Challenges and Opportunities	
9:45AM -- 10:00AM	Break	
10:00AM -- 11:00AM	**Session – 03** **Session Title: NOC/Router Design** **Session Chair:** Soumyaroop Roy, soumyaroop.roy@amd.com, AMD and Mentor Graphics, Kunal_Ganeshpure@mentor.com **Papers:** Maryam Bahmani, Abbas Sheibanyrad, Frederic Petrot, Florentine Dubois, and Paolo Durante: **A 3D-NoC Router Implementation exploiting Vertically-Partially-Connected Topologies** Vinitha Palaniveloo and Arcot Sowmya: **Formal estimation of worst case communication latency in a Network on chip** Marios Evripidou, Chrysostomos Nicopoulos, Vassos Soteriou, and Jongman Kim : **Virtualizing Virtual Channels for Increased Network-on-Chip Robustness and Upgradeability** Infall Syafalni and Tsutomu Sasao**: A Fast Head-Tail Expression Minimizer for TCAM Reduction—Application to Packet Classification**	**Session – 04** **Session Title: Thermal Analysis and 3D IC Design** **Session Chair:** Aida Todri, todri@lirmm.fr, French National Center for Scientific Research, France and Helena Silva, helena.silva@uconn.edu, University of Connecticut **Papers:** Bing Shi, Ankur Srivastava, and Avram Bar-Cohen: **Hybrid 3D-IC Cooling System Using Micro-Fluidic Cooling and Thermal TSVs** Eric Guthmuller, Ivan Miro-Panades, and Alain Greiner**: Adaptive Stackable 3D Cache Architecture for Manycores** Kunal Ganeshpure and Sandip Kundu: **Reducing Temperature Variation in 3D Integrated Circuits using Heat Pipes** Simone Corbetta, Davide Zoni, and William Fornaciari: **A Temperature and Reliability Oriented Simulation Framework for Multi-Core Architectures**
11:00AM -- 12:30PM	**Session – 05** **Session Title**: VLSI Architectures, Designs, and Implementations of Cryptographic Systems for Constrained Resources Environments **Session Chair**:	**Session – 06** **Session Title:** RRAM and Computing **Session Chairs**: Dhireesha Kudithipudi, dxkeec@rit.edu, Rochester Institute of Technology and Garrett S. Rose, garrett.rose@rl.af.mil, Airforce research

	Nicolas Sklavos, nsklavos@ieee.org, Technological Educational Institute of Patras, Greece **Papers:** Neil Hanley and Maire O'Neill: **Hardware Comparison of the ISO/IEC 29192-2 Block Ciphers** Ignacio Algredo-Badillo, Claudia Feregrino, Miguel Morales, and René Cumplido: **Throughput and Efficiency Analysis of Unrolled Hardware Architectures for the SHA-2 Family** N. Sklavos, P. Kitsos, and O. Koufopavlou: **VLSI Design and Implementation of Homophonic Security System**	Laboratory **Papers:** Rashmi Jha and Branden Long: **Understanding the Switching Mechanism in Transition Metal Oxide Based ReRAM Devices** A. Faraclas, N. Williams, F. Dirisaglik, K. Cil, A. Gokirmak, and H. Silva: **Operation dynamics of phase-change memory cells and the role of access devices** Jeyavijayan Rajendran, Garrett S. Rose, Ramesh Karri, and Miodrag Potkonjak: **Nano-PPUF: A Memristor-based Security Primitive** Ganesh Khedkar and Dhireesha Kudithipudi: **RRAM motifs for mitigating power-attacks in 3D-IC's**
12:30PM -- 2:00PM	Lunch	
2:00PM -- 3:00PM	**Session – 07** **Session Title: Logic Synthesis and Testing** **Session Chair:** Soumyaroop Roy, soumyaroop.roy@amd.com, AMD and Mahadevan Gomathisankaran, mgomathi@unt.edu, University of North Texas **Papers:** Maciej Nikodem, Marek Bawiec, and Janusz Biernat: **Synthesis of Multithreshold Threshold Gates** Yingying Zhang, Emmanuel Rodriguez, Hao Zheng, and Chris Myers: **An Improvement in Partial Order Reduction Using Behavioral Analysis** Kunal Ganeshpure and Sandip Kundu: **A DFT Methodology for Repairing**	**Session – 08** **Session Title: Advanced Circuit Design Techniques** **Session Chair:** Xiaowei Li, lxw@ict.ac.cn, Chinese Academy of Sciences, China and Helena Silva, helena.silva@uconn.edu, University of Connecticut **Papers:** Arunkumar Vijayakumar, Raghavan Kumar, and Sandip Kundu: **On Design of Low Cost Power Supply Noise Detection Sensor for Microprocessors** Arun A. Balakrishnan, V. Suresh Babu and M. R. Baiju: **Analog CMOS Implementation of Fast Fourier Transform Using Current Mirror Circuits**

	Embedded Memories of Large MPSoCs Sanga Chaki, Chandan Giri, and Hafizur Rahaman: **Binary Difference Based Test Data Compression for NoC Based SoCs**	Trivikrama Rao, Ashudeb Dutta, Shivgovind Singh, Arijit De, and Bhibu Dutta Sahoo**: A Tuneable CMOS Pulse Generator For Detecting The Cracks In Concrete Walls** Xuelian Liu and John F. McDonald: **A Wide Band Locking Range Quarter-Phase Generator PLL Using 0.13um BiCMOS Techology**
3:00PM -- 4:00PM	**Session – 09** **Session Title: Emerging Circuit Technologies** **Session Chairs:** Aida Todri, todri@lirmm.fr, French National Center for Scientific Research, France, and Ashok Srivastava, eesriv@lsu.edu, Louisiana State University **Papers:** Amlan Chakrabarti, Chiachun Lin, and Niraj Jha: **Design of Quantum Circuits for Random Walk Algorithms** Mahesh Poolakkaparambil, Jimson Mathew, and S. P. Mohanty: **An Investigation of Concurrent Error Detection over Binary Galois Fields in CNTFET and QCA Technologies** Mohsen M. Arjmand, Mohsen Soryani, Keivan Navi, and Mohammad A. Tehrani: **A Novel Ternary-to-Binary Converter in Quantum-dot Cellular Automata** Ravindhiran Mukundrajan, Matthew Cotter, Vinay Saripalli, Mary Jane Irwin, Suman Datta, and Vijaykrishnan Narayanan: **Ultra Low Power Circuit Design using Tunnel FETs**	**Session – 10** **Session Title: Hardware Security** **Session Chair:** Ambar Sarkar, ambar.sarkar@paradigm-works.com, Paradigm Works and Kunal Ganeshpure, Mentor Graphics, Kunal_Ganeshpure@mentor.com **Papers:** Apostolos Fournaris and Odysseas Koufopavlou: **Protecting CRT RSA against Fault and Power Side Channel Attacks** Raghavan Kumar, Vinay C Patil, and Sandip Kundu: **On Design of Temperature Invariant Physically Unclonable Functions based on Ring Oscillators** Domenic Forte and Ankur Srivastava: **Manipulating Manufacturing Variations for Better Silicon-Based Physically Unclonable Functions** Yuejian Fang and Zhonghai Wu: **A New Parallel Processor Architecture for Genus 2 Hyperelliptic Curve Cryptosystems**
4:00PM -- 4:15PM	Tea break	
4:15PM -- 5:00PM	**Plenary Talk – 1** Fadi Kurdahi, kurdahi@uci.edu, University of California, Irvine, Title: Application-	

	aware System Design for late and post silicon eras	
5:00PM -- 6:00PM	**Session – 11** **Session Title: Reliability and fault tolerance** **Session Chairs:** Aswin Sreedhar, aswin.sreedhar@intel.com, Intel Corporation and Jiang Xu, jiang.xu@ust.hk, The Hong Kong University of Science and Technology **Papers:** Hong Luo, Yu Wang, Yu Cao, Yuan Xie, Yuchun Ma, and Huazhong Yang: **Temporal Performance Degradation under RTN: Evaluation and Mitigation for Nanoscale Circuits** Rishad A Shafik, Bashir M. Al-Hashimi, Jimson Mathew, Dhiraj Pradhan, and Saraju Mohanty: **RAEF: A Power Normalized System-level Reliability Analysis and Estimation Framework** Tao Jin and Shuai Wang: **Aging-Aware Instruction Cache Design by Duty Cycle Balancing**	**Session – 12** **Session Title: Reversible Design technologies** **Session Chair:** Ambar Sarkar, ambar.sarkar@paradigm-works.com, Paradigm Works and Ashok Srivastava, eesriv@lsu.edu, Louisiana State University **Papers:** Chetan Vudadha, P. Sai Phaneendra, V. Sreehari, Syed Ershad Ahmed, N. Moorthy Muthukrishnan, and M. B. Srinivas: **Design of Prefix-Based Optimal Reversible Comparator** Saurabh Kotiyal, Himanshu Thapliyal, and Nagrajan Ranganathan: **Mach-Zehnder: Interferometer Based All Optical Reversible NOR Gates** Robert Wille, Mathias Soeken, Eleonora Schönborn, and Rolf Drechsler: **Circuit Line Minimization in the HDL-based Synthesis of Reversible Logic** Matthew Morrison and Nagarajan Ranganathan: **Analysis of Reversible Logic Based Sequential Computing Structures using Quantum Mechanics Principles**
6:00PM -- 6:30PM	Break	
6:30PM -- 8:30PM	Symposium Banquet	
21st August 2012 (Tuesday)		
8:00AM -- 8:30AM	Registration, Breakfast	
8:30AM -- 9:15AM	**Plenary Talk – 2** Abhijit Chatterjee, abhijit.chatterjee@ece.gatech.edu, The Georgia Institute of Technology, Title: RF/Mixed-Signal Real-Time Adaptation for Error Resilience, Low	

	Power and Performance	
9:15AM -- 10:15AM	**Session – 13** **Session Title: Datapath Design and Partitioning** **Session Chair:** Bill Bowhill, bill.bowhill@intel.com, Intel Corporation and Spyros Tragoudas, spyros@engr.siu.edu, Southern Illinois University Carbondale **Papers:** Chetan Vudadha, P. Sai Phaneendra, Syed Ershad Ahmed, V. Sreehari, N. Moorthy Muthukrishnan, and M. B. Srinivas: **Design and Analysis of Reversible Ripple, Prefix and Prefix-Ripple Hybrid Adders** Matthew Morrison, Matthew Lewandowski, and Nagarajan Ranganathan**: Design of a Tree-Based Comparator and Memory Unit Based on a Novel Reversible Logic Structures** Tung Thanh Hoang and Per Larsson-Edefors**: Data-Width-Driven Power Gating of Integer Arithmetic Circuits** Yu Jiang, Hehua Zhang, Xun Jiao, Xiaoyu Song, William N. N. Hung, Ming Gu, and Jiaguang Sun: **Uncertain Model and Algorithm for Hardware/Software Partitioning**	**Session – 14** **Session Title: Design Architecture** **Session Chair:** Xiaowei Li, lxw@ict.ac.cn, Chinese Academy of Sciences, China and Chandramouli Gopalakrishnan, Synopsys gcmouli@synopsys.com **Papers:** Venkateswaran Nagarajan, Vinesh Srinivasan, Ramsrivatsa Kannan, Prashanth Thinakaran, Rajagopal Hariharan, Bharanidharan Vasudevan, Nachiappan Chidambaram Nachiappan, Karthikeyan Palavedu Saravanan, Aswin Sridharan, Vigneshwaran Sankaran, Vignesh Adhinarayanan, V.S. Vignesh, and Ravindhiran Mukundrajan: **Compilation Accelerator on Silicon** Oliver Arnold, Benedikt Nöthen, and Gerhard Fettweis: **Instruction Set Architecture Extensions for a Dynamic Task Scheduling Unit** Venkateswaran Nagarajan, Rajagopal Hariharan, Vinesh Srinivasan, Ram Srivatsa Kannan, Prashanth Thinakaran, Vigneshwaren Sankaran, Bharanidharan Vasudevan, Ravindhiran Mukundrajan, Nachiappan Chidambaram Nachiappan, Aswin Sridharan, Karthikeyan Palavedu Saravanan, Vignesh Adhinarayanan, and Vignesh Veppur Sankaranarayanan: **SCOC IP Cores for Custom Built Supercomputing Nodes** Marco Aurelio Nuño Maganda, Miguel Arias-Estrada, Cesar Torres-Huitzil, Hector Aviles-Arriaga, Yahir Hernandez-Mier, and Miguel Morales-Sandoval: **A Hardware Architecture for Image Clustering Using Spiking Neural Networks**

10:15AM -- 11:15AM	**Session – 15** **Session Title: Analog Design** **Session Chairs:** Alex K. Jones, akjones@pitt.edu, University of Pittsburgh and Aswin Sreedhar, aswin.sreedhar@intel.com, Intel Corporation **Papers:** Geng Zheng, Saraju Mohanty, and Elias Kougianos: **Metamodel-Assisted Fast and Accurate Optimization of an OP-AMP for Biomedical Applications** Arnab Khawas and Siddhartha Mukhopadhyay: **Variance Optimization of CMOS OpAmp Performances using Experimental Design Approach** Oghenekarho Okobiah, Saraju Mohanty, Elias Kougianos, Oleg Garitselov, and Geng Zheng: **Stochastic Gradient Descent Optimization for Low Power Nanoscale CMOS Thermal Sensor Design**	**Session – 16** **Session Title:** Methodology for Efficient Multi-threading of Parsers in EDA Tools **Session Chair:** Chandramouli Gopalakrishnan, Synopsys gcmouli@synopsys.com **Papers:** Prakash Shanbag, Saibal Ghosh, and Chandramouli Gopalakrishnan, **Methodology for efficient Multi-threading in EDA Parsers** Prakash Shanbag, Saibal Ghosh, and Chandramouli Gopalakrishnan, **A Case Study in developing an efficient Multi-threaded EDA Parser - Synopsys SDF Parser**
11:15AM – 12:15PM	**Session – 17** **Session Title: Design Fabric and Microfluidic Design** **Session Chair:** Bill Bowhill, Intel Corporation, bill.bowhill@intel.com, and Alex K. Jones, akjones@pitt.edu, University of Pittsburgh **Papers:** Luca Montesi, Zeljko Zilic, Takahiro Hanyu, and Daisuke Suzuki: **Building Blocks to Use in Innovative non-Volatile FPGA Architecture Based on MTJs.** Takahiro Watanabe and Minoru Watanabe. : **0.18 um CMOS process high-sensitive differential optically reconfigurable gate array VLSI**	**Session – 18** **Session Title: Design Modeling and Analysis** **Session Chair:** Nicolas Sklavos, nsklavos@ieee.org, Technological Educational Institute of Patras, Greece and Yiyu Shi, yshi@mst.edu, Missouri Science & Technology **Papers:** Oghenekarho Okobiah, Saraju Mohanty, and Elias Kougianos**: Geostatistical-Inspired Metamodeling and Optimization of Nano-CMOS Circuits** John Lee, Puneet Gupta, and Fedor Pikus: **Parametric Hierarchy Recovery in Layout Extracted Netlists**

	Debasis Mitra, Sudip Roy, Krishnendu Chakrabarty, and Bhargab B. Bhattacharya: **On-Chip Sample Preparation with Multiple Dilutions using Digital Microfluidics** Pranab Roy, Rupam Bhattacharjee, Hafizur Rahaman and Parthasarathi Dasgupta: **A new algorithm for routing-aware net placement in cross-referencing digital microfluidic biochips**	Raul Chipana, Eduardo Chielle, Fernanda Kastensmidt, Jorge Tonfat, and Ricardo Reis**: Evaluating Circuit Error Probability Due to SET in Clock Tree Networks** Chandra Babu Dara, Themistoklis Haniotakis, and Spyros Tragoudas: **Delay Analysis for an N-Input Current Mode Threshold Logic Gate**
12:15PM -- 1:45PM	Lunch	
1:45PM -- 2:30PM	**Plenary Talk – 3** Fabio Campi, fabio.campi@st.com, ST Microelectronics, Title: The Low Power Era: Opportunities for Architecture Design	
2:30PM -- 4:00PM	**Session – 19** **Session Title:** New Techniques for Secure Embedded Systems **Session Chair:** Mahadevan Gomathisankaran, mgomathi@unt.edu, University of North Texas **Papers:** Ashok Srivastava and Rajiv Soundararajan: **Testing of Trusted CMOS Data Converters** Pei-Wen Luo, Tao Wang, Chin-Long Wey, Liang-Chia Cheng, Bih-Lan Sheu, and Yiyu Shi: **Reliable Power Delivery System Design for Three-Dimensional Integrated Circuits** Mahadevan Gomathisankaran and Akhilesh Tyagi: **A Novel Design of Secure and Private Circuits** Arun K. Kanuparthi, Ramesh Karri, Gaston Ormazabal, and Sateesh K. Addepalli: **A Survey of Microarchitecture Support for Embedded Processor Security**	**Session – 20** **Session Title:** System Innovations with Emerging Memory Technologies **Session Chair:** Vijaykrishnan Narayanan, vijay@cse.psu.edu, The Pennsylvania State University **Papers:** Xiuyuan Bi, Hai Li, and Jae-Joon Kim: **Analysis and Optimization of Thermal Effect on STT-RAM Based 3-D Stacked Cache Design** Zili Shao, Naehyuck Chang, and Nikil Dutt: **PTL: PCM Translation Layer** Hyung Gyu Lee, Seungcheol Baek, Jongman Kim, and Chrysostomos Nicopoulos: **A Compression-based Hybrid MLC/SLC Management Technique for Phase-Change Memory Systems** Matt Poremba and Yuan Xie: **NVMain: An Architectural-Level Main Memory Simulator for Emerging Non-volatile Memories**

4:00PM -- 5:30PM	**Session -- 21** **Session Title:** Hardware-Software Co-design for Emerging NVM **Session Chair:** Hai (Helen) Li, hli@poly.edu, Polytechnic Institute of NYU **Papers:** Zili Shao, Yongpan Liu, Yiran Chen, and Tao Li: **Utilizing PCM for Energy and Power Optimization in Embedded Systems** Yong Li and Alex K. Jones**: Cross-Layer Techniques for Optimizing Systems Utilizing Memories with Asymmetric Access Characteristics** Qingan Li, Liang Shi, Jianhua Li, Chun Jason Xue, and Yanxiang He: **Code Motion for Migration Minimization in STT-RAM Based Hybrid Cache**	
5:30PM -- 5:45PM	**ISVLSI 2012 Closing Remarks**	