ISVLSI 2014 Program Highlights

9th July 2014 (Wed)		
1:00PM--1:30PM	Delegate Arrival and Registration	
1:30PM --2:00PM	**Inaugural Event**	
2:00PM --3:00PM	**Session – 01 - Variation-Aware and Low-Power Design**	**Session – 02 - Hardware Security and Testing (SS)**
3:00PM --4:00PM	**Session – 03 - Advanced Circuit for Computing**	**Session – 04 - New Directions in Hardware Trust (SS)**
4:00PM --5:00PM	**Session – 05 - Memristive and 3-Dimensional Designs**	Intentionally Left Blank
5:00PM --6:00PM	**Session – 06 - Poster Session**	**Session – 07 - Ph. D. Forum**
10th July 2014 (Thu)		
8:00AM - 8:30AM	Registration, Breakfast	
8:30AM - 9:15AM	**Plenary Talk -- 1**	
9:15AM-10:15AM	**Session – 08 - Biomedical and Sensor Circuits**	**Session – 09 - Variability and Aging of Integrated Circuits (SS)**
10:15AM-11:15AM	**Session – 10 - Memory and Oscillator Circuits**	
11:15AM-12:15PM	**Session – 11 - Test Generation and Fault Diagnosis**	**Session – 12 - CAD for Verification & Debug**
12:15PM - 1:45PM	Lunch	
1:45PM --2:30PM	**Plenary Talk -- 2**	
2:30PM --3:30PM	**Session – 13 - CAD for Digital Systems**	**Session – 14 - Reaching Beyond Device Scaling: Post-CMOS Perspectives (SS)**
3:30PM --4:30PM	**Session – 15 - Sub-Power Circuit and 3D Architecture**	**Session – 16 - CAD for Emerging Memory Technologies (SS)**
4:30PM --5:30PM	**Session – 17 - FinFET and Optical Technology Based Design**	**Session – 18 – Dynamic Power Management**
5:30PM --6:00PM	Break	
6:00PM --8:00PM	**Symposium Banquet**	

11th July 2014 (Fri)		
8:00AM -- 8:30AM	Registration, Breakfast	
8:30AM -- 9:15AM	**Plenary Talk – 3**	
9:15AM --10:15AM	**Session – 19 - Security and Error Tolerance in System Architecture**	**Session – 20 - VLSI for Big Data (SS)**
10:15AM-11:15AM	**Session – 21 – Network-on-a-Chip (NoC) Based Systems**	**Session – 22 - CAD for Power Integrity**
11:15AM-12:15PM	**Session – 23 - Secure and Trustworthy Embedded Systems (SS)**	**Session – 24 - Advanced Methods for Futuristic Systems**
12:15PM - 1:45PM	Lunch	
1:45PM -- 2:30PM	**Plenary Talk -- 4**	
2:30PM - 3:30PM	**Session – 25 - High-Reliability Design**	**Session – 26 - Reaching Beyond Device Scaling: CMOS Perspectives (SS)**
3:30PM - 4:30PM	**Session – 27 - Soft Error Analysis and Mitigation**	**Session – 28 - CAD Recent Developments on Partitioning**
4:30PM -- 5:00PM	**ISVLSI Closing Remarks**	

ISVLSI 2014 Program Details

9th July 2014 (Wed)

1:00PM--1:30PM	Delegate Arrival and Registration	
1:30PM --2:00PM	**Inaugural Event**	
2:00PM --3:00PM	**Session – 01 - Variation-aware and low-power design -** Chair: Shiyan Hu - *Michigan Technological University.*	**Session – 02 - Hardware Security and Testing (SS) -** Chair: Huawei Li - *Chinese Academy of Sciences and* Xiaoqing Wen - *Kyushu Institute of Technology.*
	Variation Aware Design of Post-Silicon Tunable Clock Buffer; Vikram Suresh and Wayne Burleson - *University of Massachusetts, Amherst.*	***Design-for-Security vs. Design-for-Testability: A Case Study on DFT Chain in Cryptographic Circuits;*** Yier Jin - *University of Central Florida.*
	Framework of an Adaptive Delay-Insensitive Asynchronous Platform for Energy Efficiency; Liang Men, Brent Hollosi, and Jia Di - *University of Arkansas.*	***PUF Interfaces and their Security;*** Marten Van Dijk - *University of Connecticut*.
	Regulator-Gating Methodology with Distributed Switched Capacitor Voltage Converters; Orhun Aras Uzun and Selcuk Kose - *University of South Florida, Tampa.*	***Post-Silicon Validation and Calibration of Hardware Security Primitives;*** Xiaolin Xu, Vikram Suresh, Raghavan Kumar, and Wayne Burleson - *University of Massachusetts, Amherst.*
3:00PM --4:00PM	**Session – 03 - Advanced Circuit for Computing -** Chair: Hai (Helen) Li - *University of Pittsburgh.*	**Session – 04 - New Directions in Hardware Trust (SS) -** Chair: Ramesh Karri - *Polytechnic Institute of New York University.*
	Design of a Flexible, Energy Efficient (Auto)Correlator Block for Timing Synchronization; Fabio Campi - *Simon Fraser University, Canada,* Roberto Airoldi, and Jari Nurmi - *Tampere University of Technology, Finland.*	***A Chaos-based Arithmetic Logic Unit and Implications for Obfuscation;*** Garrett S. Rose - *Air Force Research Laboratory/RITA, Rome, USA.*
	A Novel Class of Linear MIMO Detectors With Boosted Communications Performance: Algorithm and VLSI Architecture; Dominik Auras, Rainer Leupers, and Gerd Ascheid - *RWTH Aachen University, Germany.*	***Trust no one: Thwarting "heartbleed" attacks using privacy-preserving computation;*** Nektarios Georgios Tsoutsos - *NYU Polytechnic School of Engineering* and Michail Maniatakos - *NYU Abu Dhabi.*
	Experiments with High Speed Parallel Cubing Units; Son Bui, James Stine, and Masoud Sadeghian - *Oklahoma State University.*	

4:00PM - - 5:00PM	**Session – 05 - Memristive and 3-Dimensional Designs -** Chair: Sujay Deb, *Indraprastha Institute of Information Technology Delhi (IIIT Delhi), India.*	Intentionally Left Blank
	A Weighted Sensing Scheme for ReRAM-based Cross-point Memory Array; Chenchen Liu and Hai Li - *University of Pittsburgh.*	
	FuzzRoute: A Method For Thermally Efficient Congestion Free Global Routing in 3D ICs; Debashri Roy - *Bengal Engineering and Science University, Shibpur, India,* Prasun Ghosal, Saraju Mohanty - *University of North Texas.*	
	Neuromemristive Extreme Learning Machines for Pattern Classification; Cory Merkel and Dhireesha Kudithipudi - *Rochester Institute of Technology.*	
5:00PM - - 6:00PM	**Session – 06 - Poster Session** - Chair: Saraju P. Mohanty - *University of North Texas* and Sanjukta Bhanja - *University of South Florida.*	**Session – 07 - Ph. D. Forum -** Chair: Michael Hübner - *Ruhr University Bochum, Germany.*
	A New Walsh Hadamard Transform Architecture Using Current Mode Circuit; Swagata Bhattacharya - *Guru Nanak Institute of Technology, India,* Somsubhra Talapatra - *Aliah University, India.*	***Enabling Side Channel Secure FSMs in the presence of Low Power Requirements;*** Mike Borowczak - *The University of Cincinnati,* Ranga Vemuri - *The University of Cincinnati.*
	A Transient-enhanced Capacitorless LDO Regulator With improved Error Amplifier; Suresh A, Patri Srihari Rao, KSR Krishna Prasad, and Saurabh Dixit - *NIT Warangal, India.*	***Dynamic Phase-based Optimization of Embedded Systems;*** Tosiron Adegbija - *University of Florida,* and Ann Gordon-Ross - *University of Florida.*
	Memristor Crossbar Based Programmable Interconnects; Raqibul Hasan and Tarek M. Taha - *University of Dayton.*	***A Low-Cost and High-Performance Embeded System Architecture and An Evaluation Methodology;*** Xiaokun Yang - *Florida International University and* Jean Andrian - *Florida International University.*

Automatic Handling of Conflicts in Synchronous Interpreted Time Petri Nets Implementation; Hélène Leroux - *LIRMM, France*, Karen Godary-Dejean - *LIRMM, UM2, France,* Guillaume Coppey - *MXM-AXONIC, France,* and David Andreu - *LIRMM, France.*	***Exploring Kriging for Fast and Accurate Design Optimization of Nanoscale Analog Circuits;*** Oghenekarho Okobiah - *University of North Texas*, Saraju Mohanty - *University of North Texas,* and Elias Kougianos - *University of North Texas.*
Swarm Intelligence Driven Simultaneous Adaptive Exploration of Datapath and Loop Unrolling Factor during Area-Performance Tradeoff; Anirban Sengupta and Vipul Kumar Mishra - *Indian Institute of Technology (IIT) Indore, India.*	***Exploration of Magnetic RAM based memory hierarchy for multicore architecture;*** Sophiane Senni - *LIRMM, France.*
Slicing Floorplans with Handling Symmetry and General Placement Constraints; Hongxia Zhou, Chiu-Wing Sham - *The Hong Kong Polytechnic University, Hong Kong,* and Hailong Yao - *Tsinghua University*.	***Theory, Synthesis, and Application of Adiabatic and Reversible Logic Circuits For Security Applications;*** Matthew Morrison - *University of South Florida, Tampa.*
Physical vs. Physically-Aware Estimation Flow: Case Study of Design Space Exploration of Adders; Ivan Ratkovic - *BSC, Spain,* Oscar Palomar - *Barcelona Supercomputing Center, Spain,* Milan Stanic - *Barcelona Supercomputing Center, Spain, Osman Unsal - Barcelona Supercomputing Center, Spain,* Adrian Cristal - *Barcelona Supercomputing Center, Spain,* and Mateo Valero - *BSC-Microsoft Research Center, Spain.*	Intentionally Left Blank
Data Correlation Aware Serial Encoding for Low Switching Power On-Chip Communication; Somrita Ghosh - *Bengal Engineering and Science University, Shibpur, India,* Prasun Ghosal - *University of North Texas,* Nabanita Das - *Indian Statistical Institute Kolkata, India,* Saraju Mohanty - *University of North Texas,* and Oghenekarho Okobiah - *University of North Texas.*	
Computational Architectures based on Coupled Oscillators; Matthew J. Cotter - *Pennsylvania State University,* Yan Fang, Steven P. Levitan, Donald M. Chiarulli - *University of Pittsburgh,* and Vijaykrishnan Narayanan - *The Pennsylvania State University.*	
A Low Latency Scalable 3D NoC Using BFT Topology with Table Based Uniform Routing; Avik Bose - *Bengal Engineering and Science University, Shibpur, India,* Prasun Ghosal - *University of North Texas,* and Saraju Mohanty - *University of North Texas.*	

An Algorithm for Parallel Assay Operations in a Restricted Sized Chip in Digital Microfluidics; Debasis Dhal - *Assam University, Silchar, India,* Piyali Datta - *University of Calcutta, India*, Arpan Chakrabarty - *University of Calcutta, India,* Goutam Saha - *North Eastern Hill University, India,* and Rajat Kumar Pal - *University of Calcutta, India.*
Analytical Model for Inverter Design using Floating Gate Graphene Field Effect Transistors; Atul Kumar Nishad, Aditya Dalakoti, Ashish Jindal, Rahul Kumar, Somesh Kumar, and Rohit Sharma - *IIT Ropar, India.*
Modeling the Impact of TSVs on Average Wire Length in 3DICs using a Tier-Level Hierarchical Approach; Gopi Neela and Jeffrey Draper - *University of Southern California.*
Removing the Root of Trust: Secure Oblivious Key Establishment for FPGAs; Lei Xu and Weidong Shi - *University of Houston.*
Reconfigurable Dynamic Trusted Platform Module for Control Flow Checking; Sanjeev Das - *Nanyang Technological University, Singapore,* Wei Zhang - *Hong Kong University of Science and Technology, Hong Kong,* and Yang Liu - *Nanyang Technological University, Singapore.*
Patterned Heterogeneous CMPs: The Case for Regularity-Driven System-Level Synthesis; Nikita Nikitin and Magnus Jahre - *NTNU, Norway.*
Energy-Aware Thread Scheduling for Embedded Multi-Threaded Processors: Architectural Level Design and Implementation; Mahanama Wickramasinghe and Hui Guo - *The University of New South Wales, Australia.*
An Efficient Hardware Implementation of DVFS in Multi-Core System with Wireless Network-on-Chip; Hemanta Kumar Mondal, Sri Harsha Gade, and Sujay Deb - *IIIT Delhi, India.*
A Broadcast-Enabled Sensing System for Embedded Multi-core Processors; Jia Zhao, Shiting (Justin) Lu, Wayne Burleson, and Russell Tessier - *University of Massachusetts, Amherst.*
Session Based Core Test Scheduling for 3D SOCs; Surajit Kumar Roy, Payel Ghosh, Hafizur Rahaman, and Chandan Giri - *Bengal Engineering & Science University, Shibpur, India.*
On Designing Robust Path-Delay Fault Testable Combinational Circuits based on Functional Properties; Rupali Mitra, Debesh K. Das - *Jadavpur University, India,* and Bhargab B. Bhattacharya - *Indian Statistical Institute, Kolkata, India.*
Cost-Effective Test Optimized Scheme of TSV-Based 3D SoCs for Pre-bond Test; Kele Shen, Dong Xiang, and Zhou Jiang - *Tsinghua University, China.*
Impact of Process Variations on Reliability and Performance of 32-nm 6T SRAM at Near Threshold Voltage; Lingbo Kou and William Robinson - *Vanderbilt University.*
A Low-power Enhanced Bitmask-dictionary Scheme for Test Data Compression; Vahid Janfaza, Payman Behnam, Bahjat Forouzandeh, and Bijan Alizadeh - *University of Tehran, Iran.*
A Delay Probability Metric for Input Pattern Ranking Under Process Variation and Supply Noise; Anu Asokan, Aida Todri-Sanial, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, and Arnaud Virazel - *LIRMM-University of Montpellier II/CNRS, France.*

10th July 2014 (Thu)		
8:00AM -- 8:30AM	Registration, Breakfast	
8:30AM -- 9:15AM	**Plenary Talk -- 1** **Title: Variability-Resistant HW/SW Stack Through Improved Sensing** **Speaker:** Rajesh K. Gupta, University of California, San Diego **Chair**: N. Ranganathan, University of South Florida	
9:15AM -- 10:15AM	**Session – 08 - Biomedical and sensor circuits -** Chair: Selçuk Köse, *University of South Florida.*	**Session – 09 - Variability and Aging of Integrated Circuits (SS) -** Chair: Xin Li, *Carnegie Mellon University* and Jose Pineda de Gyvez, *NXP Semiconductors.*
	A Low-Noise Variable-Gain Amplifier for in-Probe 3D Imaging Applications Based on CMUT Transducers; Hourieh Atarzadeh and Trond Ytterdal - *NTNU, Norway.*	***Variation-aware Analysis and Test Pattern Generation Based on Functional Faults;*** Masahiro Fujita - *University of Tokyo, Japan.*
	A CMOS Temperature Sensor with -0.34°C to 0.27°C Inaccuracy from -30°C to 80°C; Hai Chi and Tom Chen - *Colorado State University.*	***Where is the Achilles Heel under Circuit Aging;*** Ketul Sutaria, Athul Ramkumar, Rongjun Zhu, and Yu Cao - *Arizona State University.*
	A Compact CMOS Ring Oscillator with Temperature and Supply Compensation for Sensor Applications; Yanmei Wang, Pak Kwong Chan, and King Ho Li - *Nanyang Technological University, Singapore.*	
10:15AM -- 11:15AM	**Session – 10 - Memory and Oscillator circuits -** Chair: Jia Di, *University of Arkansas.*	**Session 09 -** *Contd.*
	FinCACTI: Architectural Analysis and Modeling of Caches with Deeply-scaled FinFET Devices; Alireza Shafaei, Yanzhi Wang, Xue Lin, and Massoud Pedram – *University of Southern California.*	***Chip Health Monitoring Using Machine Learning;*** Farshad Firouzi - *Karlsruhe Institute of Technology, Germany,* Fangming Ye, Krishnendu Chakrabarty - *Duke University,* and Mehdi B. Tahoori - *Karlsruhe Institute of Technology, Germany.*
	Independently-Controlled-Gate FinFET 6T SRAM Cell Design for Leakage Current Reduction and Enhanced Read Access Speed; Kaisheng Ma, Huichu Liu, Yang Xiao, Yang Zheng, Xueqing Li, Sumeet Kumar Gupta, Yuan Xie, and Vijaykrishnan Narayanan - *Pennsylvania State University.*	***Toward Holistic Modeling, Margining and Tolerance of IC Variability;*** Andrew B. Kahng - *University of California, San Diego.*

	A Low-Voltage Low-Power LC Oscillator Using the Diode-Connected SymFET; Xueqing Li, Wei-Yu Tsai, Huichu Liu, Suman Datta, and Vijaykrishnan Narayanan - *Pennsylvania State University.*	
11:15AM – 12:15PM	**Session – 11 - Test Generation and Fault Diagnosis -** Chair: Wei Wang, *Hefei University of Technology* and Russell Tessier, *University of Massachusetts, Amherst*.	**Session – 12 - CAD for Verification & Debug -** Chair: Pierre-Emmanuel Gaillardon - *EPFL, Lausanne, Switzerland* and Chandan Giri - *Indian Institute of Engineering Science & Technology, Shibpur, India*.
	FDPIC: Generation of Functional Test Sequences Based on Fault-Dependent Primary Input Cubes; Irith Pomeranz - *Purdue University.*	***Layout-aware Selection of Trace Signals for Post-Silicon Debug;*** Prateek Thakyal and Prabhat Mishra - *University of Florida.*
	OBO: An Output-By-Output Scoring Algorithm for Fault Diagnosis; Irith Pomeranz - *Purdue University.*	***Configurable Architecture for Double / Two-Parallel Single Precision Floating Point Division;*** Manish Kumar Jaiswal, Ray C.C. Cheung - *City University of Hong Kong, Hong Kong,* M. Balakrishnan, and Kolin Paul - *IIT Delhi, India.*
	Diagnosis of Gate Delay Faults in the Presence of Clock Delay Faults; Yoshinobu Higami, Hiroshi Takahashi, Shin-Ya Kobayashi - *Ehime University, Japan,* and Kewal K. Saluja – *University of Wisconsin, Madison.*	***Effective Combination of Algebraic Techniques and Decision Diagrams to Formally Verify Large Arithmetic Circuits;*** Farimah Farahmandi - *University of Florida,* Bijan Alizadeh, and Zain Navabi - *University of Tehran, Iran.*
12:15PM -- 1:45PM	Lunch	
1:45PM -- 2:30PM	**Plenary Talk -- 2** **Title: Exploring the Beyond CMOS Options for Energy Efficient Computation** **Speaker:** Ian A. Young, Intel Corporation **Chair**: Sanjukta Bhanja, University of South Florida	
2:30PM -- 3:30PM	**Session – 13 - CAD for Digital Systems -** Chair: Hao Zheng - *University of South Florida* and Nicolas Sklavos - *Technological Educational Institute of Western Greece, Greece.*	**Session – 14 - Reaching Beyond Device Scaling: Post-CMOS Perspectives (SS) -** Chair: Ashok Srivastava - *Louisiana State University*

	Improving GA-based NoC mapping algorithms using a formal model; Vinitha Arakkonam Palaniveloo, Jude Angelo Ambrose, and Arcot Sowmya - *University of New South Wales, Australia.*	***Buffering Single-Walled Carbon Nanotubes Bundle Interconnects for Timing Optimization;*** Lin Liu, Yuchen Zhou, and Shiyan Hu - *Michigan Technological University, Houghton.*
	Simultaneous Two-Dimensional Cell Layout Compaction Using MILP with ASTRAN; Adriel Mota Ziesemer Junior, and Ricardo Augusto da Luz Reis - *UFRGS, Brazil.*	***Characterization of MWCNT VLSI Interconnects with Self-heating Induced Scatterings;*** K. M. Mohsin, Ashok Srivastava - *Louisiana State University,* Ashwani K. Sharma, and Clay Mayberry - *Air Force Research Laboratory, KAFB.*
	Function Extraction from Arithmetic Bit-level Circuits; Maciej Ciesielski, Walter Brown, Duo Liu - *University of Massachusetts Amherst,* and Andre Rossi - *Universite de Breatagne Sud, Lorient, France.*	***High Mobility n and p Channels on Gallium Arsenide and Silicon Substrates using Interfacial Misfit Dislocation Arrays;*** Darryl Shima and Ganesh Balakrishnan - *University of New Mexico.*
3:30PM - - 4:30PM	**Session – 15 - Sub-Power Circuit and 3D Architecture -** Chair: Yoshinobu Higami, *Ehime University* and William H. Robinson, *Vanderbilt University*.	**Session – 16 - CAD for Emerging Memory Technologies (SS) -** Chair: Aida Todri-Sanial, *CNRS – LIRMM / Université Montpellier 2, France* and Vasilis Pavlidis – *University of Manchester, UK*.
	Linear Compositional Delay Model for the Timing Analysis of Sub-Powered Combinational Circuits; Jiaoyan Chen, Christian Spagnol, Satish Grandhi, Emanuel Popovici - *University College Cork, Ireland,* Sorin Cotofana - *Delft University of Technology, Netherlands,* and *Alexandru Amaricai - Universitatea Politehnica Timisoara, Ireland.*	***Computing with Spin-Transfer-Torque Devices: Prospects and Perspectives;*** Kaushik Roy, Mrigank Sharad, Deliang Fan, and Karthik Yogendra - *Purdue University*.
	2D to 3D Test Pattern Retargeting using IEEE P1687 based 3D DFT Architectures; Yassine Fkih - *LIRMM/CEA, France,* Pascal Vivet - *CEA-LETI, France,* Bruno Rouzeyre - *LIRMM. Univ. Montpellier 2, France,* Marie-Lise Flottes - *LIRMM, France,* Giorgio Di Natale - *LIRMM, France,* and Juergen Schloeffel - *Mentor Graphics, Germany.*	***Unlocking Controllable-Polariy Transistors Opportunities by Exclusive OR and Majority Logic Synthesis;*** Pierre-Emmanuel Gaillardon, Luca Gaetano Amarù, and Giovanni De Micheli - *EPFL, Switzerland*.

	HARS : A High-Performance Reliable Routing Scheme for 3D NoCs; Jun Zhou, Huawei Li - *Institute of Computing Technology, Chinese Academy of Sciences, China,* Yuntan Fang - *Institute of Computing Technology, Chinese Academy of Sciences & Swiss Federal Institute of Technology in Lausanne, China,* Tiancheng Wang - *Institute of Computing Technology, Chinese Academy of Sciences, China,* Yuanqing Cheng - *Beihang University, China,* and Xiaowei Li - *Institute of Computing Technology, Chinese Academy of Sciences, China.*	***Memristor Modeling — Static, Statistical, and Stochastic Methodologies;*** Hai (Helen) Li, Miao Hu - *University of Pittsburgh*, Chuandong Li and Shukai Duan - *Southwest University.*
4:30PM - - 5:30PM	**Session – 17 - FinFET and Optical Technology Based Design -** Chair: Garrett S. Rose - *Air Force Research Laboratory/RITA, Rome, USA* and Nezih Pala - *Florida International University*.	**Session – 18 – Dynamic Power Management -** Chair: Dhireesha Kudithipudi - *Rochester Institute of Technology* and Jia Di - *University of Arkansas.*
	Mach-Zehnder Interferometer based all Optical Reversible Carry-Lookahead Adder; Pratik Dutta, Chandan Bandyopadhyay, Chandan Giri, and Hafizur Rahaman - *Bengal Engineering and Science University, Shibpur, India.*	***A Feedback, Runtime Technique for Scaling the Frequency in GPU Architectures;*** Yue Wang and Nagarajan Ranganathan - *University of South Florida, Tampa.*
	Perfomance Improvement with Dedicated Transistor Sizing for MOSFET and FinFET Devices; Gracieli Posser - *Universidade Federal do Rio Grande do Sul, Brazil,* Jozeanne Belomo, Cristina Meinhardt, and Ricardo Reis - *UFRGS, Brazil.*	***Reducing Energy per Instruction via Dynamic Resource Allocation and Voltage and Frequency Adaptation in Asymmetric Multicores;*** Arunachalam Annamalai - *Advanced Micro Devices,* Rance Rodrigues - *Nvidia Corporation,* Israel Koren, and Sandip Kundu - *University of Massachusetts, Amherst.*
	5nm FinFET Standard Cell Library Optimization and Circuit Synthesis in Near- and Super-Threshold Voltage Regimes; Qing Xie, Xue Lin, Yanzhi Wang, Mohammad Javad Dousti, Alireza Shafaei, Majid Ghasemi-Gol, and Massoud Pedram - *University of Southern California.*	***System-Level Power and Energy Estimation Methodology for Open Multimedia Applications Platforms;*** Santhosh Kumar Rethinagiri, Oscar Palomar, Javier Arias Moreno, Osman Unsal, Adrian Cristal, - *BSC-Microsoft Research Center, Spain,* and Morteza Biglari-Abhari - *University of Auckland.*
5:30PM - - 6:00PM	Break	
6:00PM - - 8:00PM	**Symposium Banquet**	

11th July 2014 (Fri)		
8:00AM -- 8:30AM	Registration, Breakfast	
8:30AM -- 9:15AM	**Plenary Talk – 3** **Title: Novel Low Power Transistors in 2D Dirac Materials: Graphene and Topological Insulators** **Speaker:** Sanjay Banerjee, University of Texas at Austin **Chair**: Manuel D'Abreu, SanDisk Corporation	
9:15AM -- 10:15AM	**Session – 19 - Security and Error Tolerance in System Architecture -** Chair: Sanjukta Bhanja - *University of South Florida, Tampa.*	**Session – 20 - VLSI for Big Data (SS) -** Chair: Theocharis Theocharides, *University of Cyprus, Cyprus* and Madhu Mutyam, *Indian Institute of Technology, Madras, India.*
	Robustness Analysis of Real-Time Scheduling Against Differential Power Analysis Attacks; Ke Jiang - *Linköping University, Sweden,* Lejla Batina - *Radboud University Nijmegen, Netherlands,* Petru Eles, and Zebo Peng - *Linköping University, Sweden.*	***Achieving High-Performance Video Analytics with Lightweight Cores and a Sea of Hardware Accelerators;*** Kevin M. Irick - *SiliconScapes LLC, USA,* and Nandhini Chandramoorthy, *Pennsylvania State University.*
	Moving Network Protection from Software to Hardware: an Energy Efficiency Analysis; André Luiz Pereira de França, Ricardo Pereira Jasinski, Volnei Antonio Pedroni - *UTFPR, Brazil,* and Altair Olivo Santin - *PUCPR, Brazil*.	***Low Power and Scalable Many-Core Architecture for Big-Data Stream Computing;*** Karim Kanoun, Martino Ruggiero, David Atienza - *EPFL, Switzerland,* and Mihaela Van der Schar, *University of California, Los Angeles.*
		***Big Data Processing with FPGA Supercomputers: Opportunities and Challenges*;** Apostolos Dollas - *Technical University of Crete, GREECE.*
10:15AM -- 11:15AM	**Session – 21 - Network-on-a-Chip (NoC) Based Systems -** Chair: Prasun Ghosal, *University of North Texas & Indian Institute of Engineering Science and Technology, Shibpur, India*.	**Session – 22 - CAD for Power Integrity -** Chair: Theocharis Theocharides, *University of Cyprus, Cyprus*
	A Case Study on the Communication and Computation Behaviors of Real Applications in NoC-based MPSoCs; Zhe Wang, Weichen Liu, Jiang Xu - *HKUST, Hong Kong,* Bin Li, Ravi Iyer, Ramesh Illikkal - *Intel, USA,* Xiaowen Wu, Wai Ho Mow, and Wenjing Ye - *HKUST, Hong Kong.*	***High Performance Low Swing Clock Tree Synthesis with Custom D Flip-Flop Design;*** Can Sitik, Leo Flippini - *Drexel University,* Emre Salman - *Stony Brook University,* and Baris Taskin - *Drexel University.*

	Network-on-Chip Design for Heterogeneous Multiprocessor System-on-Chip; Bharath Phanibhushana and Sandip Kundu - *University of Massachusetts, Amherst.*	***Glitch Power Reduction via Clock Skew Scheduling;*** Arunkumar Vijayakumar and Sandip Kundu - *University of Massachusetts, Amherst.*
	Towards an Effective Utilization of Partially Defected Interconnections in 2D Mesh NoCs; Changlin Chen - *TU Delft, Netherlands* and Sorin D. Cotofana - *Delft University of Technology, Netherlands.*	***On maximizing decoupling capacitance of clock-gated logic for robust power delivery;*** Arunkumar Vijayakumar, Vinay C Patil and Sandip Kundu - *University of Massachusetts, Amherst.*
11:15AM – 12:15PM	**Session – 23 - Secure and Trustworthy Embedded Systems (SS) -** Chair: Mahadevan Gomathisankaran, *University of North Texas.*	**Session – 24 - Advanced Methods for Futuristic Systems -** Chair: Sandip Kundu, *University of Massachusetts, Amherst.*
	Towards Secure Analog Designs: A Secure Sense Amplifier Using Memristors; David H. K. Hoe - *The University of Texas at Tyler,* Jeyavijayan Rajendran - *New York University,* and Ramesh Karri - *Polytechnic Institute of New York University.*	***LastingNVCache: A Technique for Improving the Lifetime of Non-volatile Caches;*** Sparsh Mittal - *Oak Ridge National Laboratory, USA,* Jeffrey S. Vetter - *ORNL and Georgia Tech,* and Dong Li - *Oak Ridge National Laboratory, USA.*
	Glitch Resistant Private Circuits Design using HORNS; Mahadevan Gomathisankaran - *University of North Texas* and Akhilesh Tyagi - *Iowa State University*.	***A Reconfigurable Architecture for QR Decomposition Using A Hybrid Approach;*** Xinying Wang, Phillip Jones, and Joseph Zambreno - *Iowa State University.*
	Towards Making Private Circuits Practical: DPA Resistant Private Circuits; Jungmin Park - *Iowa State University* and Akhilesh Tyagi - *Iowa State University*.	***An Improved Thermal Model for Static Optimization of Application Mapping and Scheduling in Multiprocessor System-on-Chip;*** Juan Yi, Weichen Liu, Weiwen Jiang - *Chongqing University, China,* Mingwen Qin, - *The Hong Kong Polytechnic University, Hong Kong,* Lei Yang, Duo Liu, Chunming Xiao, Luelue Du, and Edwin H. M. Sha - *Chongqing University, China.*
12:15PM -- 1:45PM	Lunch	
1:45PM -- 2:30PM	**Plenary Talk -- 4** **Title: Some Future Dimensions in Scaling** **Speaker:** Phil Emma, IBM Thomas J. Watson Research Center, NY **Chair**: Saraju P. Mohanty, University of North Texas	

2:30PM - - 3:30PM	**Session – 25 - High-Reliability Design -** Chair: Yier Jin, *University of Central Florida* and Santhosh Kumar Rethinagiri, *BSC-Microsoft Research Center.*	**Session – 26 - Reaching Beyond Device Scaling: CMOS Perspectives (SS) -** Chair: Shiyan Hu, *Michigan Technological University*
	Impact of Cluster Size on Routability, Testability and Robustness of a Cluster in a Mesh FPGA; Saif Ur Rehman - *TIMA Laboratory, France,* Adrien Blanchardon - *Sorbonne University, France,* Arwa Ben Dhia - *Institut TELECOM, France,* Mounir Benabdenbi - *TIMA Laboratory, France,* Roselyne Chotin-Avot - *Sorbonne University, France,* Lirida Naviner - *Institut TELECOM, France,* Lorena Anghel - *TIMA Laboratory, France,* Habib Mehrez - *Sorbonne University, France,* Emna Amouri - *Institut TELECOM, France,* and Zied Marrakchi - *FLEXRAS Technologies, France.*	***"Green" On-Chip Inductors in Three-Dimensional Integrated Circuits;*** Umamaheswara Rao Tida, Varun Mittapalli - *Missouri University of Science and Technology,* Cheng Zhuo - *Intel, USA,* and Yiyu Shi - *Missouri University of Science and Technology.*
	SET Susceptibility Analysis of Clock Tree and Clock Mesh Topologies; Raul Chipana - *UFRGS, Brazil* and Fernanda Lima Kastensmidt - *Universidade Federal do Rio Grande do Sul - UFRGS, Brazil.*	***Mitigating NBTI Degradation on FinFET GPUs through Exploiting Device Heterogeneity;*** Ying Zhang, Sui Chen, Lu Peng, and Shaoming Chen - *Louisiana State University.*
	Processor Design with Asymmetric Reliability; Zheng Wang - *RWTH-Aachen University, Germany,* Goutam Paul - *Indian Statistical Institute Kolkata, India,* and Anupam Chattopadhyay - *RWTH Aachen University, Germany.*	***Multi-level, Memory-based Logic using CMOS Technology;*** Indira Priyadarshini Dugganapally, Steve E. Watkins - *Missouri University of Science and Technology,* and Benjamin Cooper - *CMC Technologies.*
3:30PM - - 4:30PM	**Session – 27 - Soft Error Analysis and Mitigation -** Chair: Fabio Campi, *Simon Fraser University* and Dominik Auras, *RWTH Aachen University*.	**Session – 28 - CAD recent developments on Partitioning -** Chair: Aida Todri-Sanial - *LIRMM/CNRS, France* and Patrick Girard - *LIRMM/CNRS, France.*
	Alternative Standard Cell Placement Strategies for Single-Event Multiple-Transient Mitigation; Bradley T. Kiddie and William H. Robinson - *Vanderbilt University.*	***A Fast Hypergraph Bipartitioning Algorithm;*** Wenzan Cai - *CUHK, Hong Kong,* Evangeline F. Y. Young - *The Chinese University of Hong Kong, Hong Kong.*

	Methodical Design Approaches to Radiation Effects Analysis and Mitigation in Flip-flop Circuits; Lawrence T. Clark and Sandeep Shambhulingaiah - *Arizona State University.*	***A Graph-Based 3D IC Partitioning Technique;*** Sabyasachee Banerjee, Subhashis Majumder - *Heritage Institute of Technology, India,* and Bhargab B. Bhattacharya - *ISI Kolkata, India.*
	Low Power Soft Error Tolerant Macro Synchronous Micro Asynchronous Pipeline; Faiq Khalid Lodhi - *NUST SEECS, Pakistan,* Syed Rafay Hasan - *Tennessee Tech University, USA,* Osman Hasan - *National University of Sciences and Technology (NUST), Pakistan,* Falah Awwad - *United Arab Emirates University, UAE.*	***Parallel Multi-core Verilog HDL Simulation using Domain Partitioning;*** Tariq B. Ahmad and Maciej Ciesielski - *University of Massachusetts, Amherst.*
4:30PM - - 5:00PM	**ISVLSI Closing Remarks**	