ISVLSI 2016 Program Outline

10 July (Sunday)	5:00 PM - 6:00 PM	**Onsite Registration**	
	6:00 PM - 8:00 PM	**Welcome Reception/Cocktail** **(Sporsored by IEEE CEDA PA Chapter)** *Roof Terrace*	
11 July 2016 (Monday)	8:00 AM - 8:30 AM	**Registration & Refreshment** *(Ballroom B)*	
	8:30 AM - 9:00 AM	**Inaugural Event** *(Ballroom B)*	
	9:00 AM - 9:45 AM	**Keynote # 1** *(Ballroom B)*	
	9:45 AM - 10:00 AM	**Coffee Break** *(Conf. Room A)*	**Coffee Break** *(Gold Room)*
	10:00 AM - 11:00 AM	Session 01: Analog and Mixed Signal I	Session 02: Special Session: FPGA Based Computing: Evolving Applications and Design Tools
	11:00 AM - 12:00 PM	Session 03: Computer Aided Design and Verification I	Session 04: Special Session: Cyber-Physical Systems: Architecture and Security in Smart Buildings and Autonomous Driving
	12:00 PM - 1:00 PM	**Lunch** *(Ballroom A)*	
	1:00 PM - 2:00 PM	**Panel Discussion** *(Ballroom A)*	
	2:00 PM - 2:30 PM	**Coffee Break** *(Conf. Room A)*	**Coffee Break** *(Gold Room)*
	2:30 PM - 3:30 PM	Session 05: Digital Circuit Design and FPGA Based Designs I	Session 06: Special Session: From Neural Science to Neuromorphic Computing
	3:30 PM - 4:30 PM	Session 07: Emerging and Post-CMOS Technologies I	Session 08: Special Session: Emerging Stochastic Computing: From Arithmetic to Applications
	4:30 PM - 4:45 PM	**Coffee Break** *(Conf. Room A)*	**Coffee Break** *(Gold Room)*
	4:45 PM - 5:45 PM	Session 09: System Design and Security I	Session 10: Testing, Reliability, and Fault-Tolerance I
	5:45 PM - 6:15 PM	**Coffee Break**	**ISVLSI Committee Meeting** *(Ivy Room)*
	6:15 PM - 9:00 PM	**Banquet Dinner** (*Grand Concourse*)	
12 July 2016 (Tuesday)	8:30 AM - 9:00 AM	**Refreshment** *(Ballroom B)*	
	9:00 AM - 9:45 AM	**Keynote # 2** *(Ballroom B)*	
	9:45 AM - 10:00 AM	**Coffee Break** *(Conf. Room A)*	**Coffee Break** *(Gold Room)*
	10:00 AM - 11:00 AM	Session 11: Digital Circuit Design and FPGA Based Designs II	Session 12: Special Session: Emerging Devices for Hardware Security: Fiction or Future
	11:00 AM - 12:00 PM	Session 13: System Design and Security II	Session 14: Special Session: The Smart-Everything Era
	12:00 PM - 1:00 PM	**Lunch** *(Ballroom A)*	
	1:00 PM - 1:45 PM	**Luncheon Keynote** *(Ballroom A)*	
	1:45 PM - 2:15 PM	**Coffee Break**	**IEEE-CS TCVLSI Meeting** *(Ivy Room)*
	2:15 PM - 3:15 PM	Session 15: System Design and Security III	Session 16: Emerging and Post-CMOS Technologies II
	3:15 PM - 4:15 PM	Session 17: Computer Aided Design and Verification II	Session 18: Special Session: Explorations in Energy Efficient Computing from Circuits to Systems
	4:15 PM - 4:30 PM	**Coffee Break** *(Conf. Room A)*	**Coffee Break** *(Gold Room)*
	4:30 PM - 5:50 PM	Session 19: Digital Circuit Design and FPGA Based Designs II	Session 20: Analog and Mixed Signal II
	5:50 PM - 6:50 PM	**Poster Session & Light Snack** *(Ballroom B)*	
	6:50 PM - 8:50 PM	**Trolley City Tour**	
13 July 2016 (Wednesday)	8:30 AM - 9:00 AM	**Refreshment** *(Ballroom B)*	
	9:00 AM - 9:45 AM	**Keynote # 3** *(Ballroom B)*	
	9:45 AM - 10:00 AM	**Coffee Break** *(Conf. Room A)*	**Coffee Break** *(Gold Room)*
	10:00 AM - 11:00 AM	Session 21: System Design and Security IV	Session 22: Special Session: Technology-aware Mapping of Algorithm to Architecture for Power, Performance, and Reliability
	11:00 AM - 12:00 PM	Session 23: Emerging and Post-CMOS Technologies III	Session 24: Special Session: Scalable Design Approach
	12:00 PM - 1:00 PM	**Lunch & Luncheon Keynote** *(Ballroom B)*	
	1:00 PM - 2:00 PM	Session 25: Computer Aided Design and Design Methodologies	Session 26: Digital Circuit Design and FPGA Based Designs III
	2:00 PM - 3:00 PM	Session 27: Digital Circuit Design and FPGA Based Designs IV	Session 28: Testing, Reliability, and Fault-Tolerance II
	3:00 PM - 3:30 PM	**Closing Remarks and Award Ceremony** *(Ballroom B)*	

KEYNOTE 1

9:00am ~ 9:45am, Monday July 11, 2016

Ballroom B

"Putting the Star in EDA, E*A"

Sani R. Nassif

CEO, Radyalis LLC

Summary: No fields in Engineering have had the sustained exponential that was Moore's Law. One of the outcomes is a rich culture of "using computers to automate the design of computers", namely EDA, which has had to rapidly adapt to ever larger complexity. But with Moore's era now over, it is time to apply the energy of the EDA community to other areas. This talk will explore the application of EDA techniques and knowhow to the area of Cancer Radiation Therapy.

About Sani R. Nassif

Sani received his Bachelors degree with Honors from the American University of Beirut in 1980, and his Masters and PhD degrees from Carnegie-Mellon University in 1981 and 1986 respectively. He then worked for ten years at Bell Laboratories in the general area of technology CAD, focusing on various aspects of design and technology coupling including device modeling, parameter extraction, worst case analysis, design optimization and circuit simulation. While at Bell Labs, working under Larry Nagel -the original author of Spice, he led a large team in the development of an in-house circuit simulator, named Celerity, which became the main circuit simulation tool at Bell Labs. In January 1996, he joined the then newly formed IBM Austin Research Laboratory (ARL), which was founded with a specific focus on research for the support of IBM's Power computer systems. After twelve years of management, he stepped down to focus on technical work again with an emphasis on applying techniques developed in the VLSI-EDA area to IBM's Smarter Planet initiative. In January 2014 Sani founded Radyalis, a company focused on applying VLSI-EDA techniques to the field of Cancer Radiation Therapy. In October 2015, Radyalis announced that it has closed a deal with LSI software to license its flagship Monte Carlo particle therapy simulator. Sani has authored one book, many book chapters, and numerous conference and journal publications. He has delivered many tutorials at top conferences and has received Best Paper awards from TCAD, ICCAD, DAC, ISQED, ICCD and SEMICON, authored invited papers to ISSCC, IEDM, IRPS, ISLPED, HOTCHIPS, and CICC. He has given Keynote and Plenary presentations at Sasimi, ESSCIRC, BMAS, SISPAD, SEMICON, VLSI-SOC, PATMOS, NMI, ASAP, GLVLSI, TAU, and ISVLSI. He is an IEEE Fellow, was a member of the IBM Academy of Technology, a member of the ACM and the AAAS, and an IBM master inventor with more than 75 patents. Dr. Nassif was the president of the IEEE Council on EDA (CEDA) for 2014 and 2015, was the General chair of the ICCAD conference in 2008, and has served on the technical program committees of ICCAD, DAC and other conferences. He received the Penrose award (given to one outstanding graduate from the American University of Beirut), the Distinguished Member of Technical Staff award from Bell Labs, three Research Accomplishment Awards from IBM, and the SRC Mahboob-Khan Outstanding Mentor awards from the SRC.

KEYNOTE 2

9:00am ~ 9:45am, Tuesday July 12, 2016

Ballroom B

Lithography-Aware Physical Design

Martin D. F. Wong

Professor, Executive Associate Dean, College of Engineering
Department of Electrical and Computer Engineering
University of Illinois at Urbana-Champaign

Summary

Lithography continues to be the backbone of circuit fabrication. In advanced IC technology nodes (20nm and beyond), manufacturing (i.e., lithography) has become the bottleneck for the chip design process. Design for manufacturing (DFM) is no longer an option but a necessity. Since physical design determines the locations and geometries of all the transistors and wires, it must understand the down-stream lithography process so that the layout patterns generated are printable on silicon. This is a challenging problem and the requirements oftentimes are non-intuitive to the designers. In this talk, we give an overview of our work on lithography-aware physical design for several leading next-generation lithography (NGL) technologies. The NGL technologies we consider include triple-patterning lithography (TPL), self-aligned double patterning (SADP), directed self-assembly (DSA) and extreme ultraviolet (EUV) lithography.

About Martin D. F. Wong

Martin D. F. Wong is the Executive Associate Dean of the College of Engineering in the University of Illinois at Urbana-Champaign (UIUC). He is also the Edward C. Jordan Professor of Electrical and Computer Engineering. He received his Ph.D. in computer science from UIUC in 1987. Prof. Wong is internationally known for his research on computer-aided design (CAD) methods for very-large-scale integrated circuits. He has published over 450 technical papers and graduated more than 46 Ph.D. students. He is a Fellow of IEEE.

LUNCHEON KEYNOTE

1:00pm ~ 1:45pm, Tuesday July 12, 2016

Ballroom A

Advanced Node Layout: Challenges and Opportunities for VLSI Design Automation

Elias Fallon

Engineering Group Director
Virtuoso R&D
Cadence Design Systems, Inc.

Summary

The introduction of FinFET devices plus multi-patterning technologies on routing layers had led to exciting changes in layout methodologies, especially in custom and analog layout design. While these technologies allow Moore's Law to continue its march through 16nm/14nm/10nm/7nm, they require drastic changes to how layout is created. The Virtuoso R&D team has been partnering with many leading customers, IP development teams, and semiconductor foundries in the past 5 years to address these challenges. The two factors of design productivity and technology challenges have led to many exciting new capabilities and methodologies for layout designers enabled by Virtuoso.

About Elias Fallon

Elias Fallon has been involved in the automation of analog circuit layout for more than 18 years, starting as one of the original employees of Neolinear, Inc. As one of the primary authors of NeoCell, a product to automate the placement and routing of analog circuits and macros, he co-developed several patented innovations. Since Neolinear's acquisition by Cadence in 2004, he has managed Virtuoso layout R&D teams focused on Analog Placement, Modgens, and other layout automation tools, as well as continuing innovative development for custom and analog layout methodologies. Beyond his work developing electronic design automation tools, he has led software quality improvement initiatives within Cadence, partnering with the Carnegie Mellon Software Engineering Institute. He is currently the Engineering Group Director leading the R&D teams responsible for the Virtuoso automated placement and routing product lines. Elias graduated from Carnegie Mellon University with an M.S. and B.S. in Electrical and Computer Engineering.

KEYNOTE 3

9:00am ~ 9:45am, Wednesday July 13, 2016

Ballroom B

Open Innovation, Diving into the deep blue sea of IOT

Xianfeng (Sean) Ding

Chief Scientist of sensing solution lab
Huawei Technologies Co., Ltd

Summary

Huawei is world leading innovator in IOT application, Huawei is pushing forward the integration of sensor, algorithm, and software for new wearable, smart home, smart car application. Motion sensor, vital sign sensor are key technology powering the wearable, which will power the entire mobile health industry, which will come trillion RMB business. Huawei like to share the progress we did so far, and call upon the whole industry to join force to innovate in this area, and completely disrupt the health industry, and enrich human life with better quality and longer life span.

About Xianfeng (Sean) Ding

Since Nov 2014, Sean serves as chief scientist for sensing solution lab, and lead the innovation for next generation of internet of things and smart phone in Huawei corporate RD team. Prior Huawei, Sean worked in sensing and control industry 15 years in silicon valley, including STMicro, Bosch sensortec, both are world top 3 sensor companies in the world. Sean also worked for Intel as principal engineer on artificial intelligence, activity recognition, and context awareness. He possesses in depth knowledge in sensing system, including physical design of MEMS and sensor, circuitry, algorithm optimization, system implementation.

LUNCHEON KEYNOTE

12:00pm ~ 12:45pm, Wednesday July 13, 2016

Ballroom A

Smart Campus – A Vision of the Future Intelligent and Connected Buildings

Charles Shelton

Senior Research Engineer
Bosch Research and Technology Center

Summary

The Internet of Things (IoT) promises to have an enormous impact on all aspects of modern life. In particular, buildings, which already have many unconnected sensors and actuators for lighting, climate control, safety and security, will become fully connected networks of sensors, actuators, devices, and computing centers that will manage and coordinate building functions. The goal of this drive towards connectivity is to improve building energy efficiency and optimize maintenance costs, while at the same time optimizing the user experience of the building occupants. We present Smart Campus, a joint research project between Bosch and Carnegie Mellon University for developing a framework and living laboratory for developing intelligent and connected building applications. This talk will explore the potential for future connected building use cases, and some of the work we have already done in deploying fully connected networks of wireless sensors in buildings for environmental monitoring, occupancy sensing, and indoor localization.

About Charles Shelton

Charles Shelton is a Senior Research Engineer at the Bosch Research and Technology Center (RTC) in Pittsburgh, PA. He is currently leading the Bosch RTC Smart Campus project. The Smart Campus project focuses on developing IoT platforms and applications for smart infrastructure and intelligent buildings. He has worked on several research projects over the years in the areas of software architecture, distributed systems, and designing graceful degradation and dependability into embedded systems for automotive electronics and building security systems. Most recently he has worked on developing software infrastructures for Internet-connected wireless sensor networks. He earned his PhD in Computer Engineering from Carnegie Mellon University (CMU) in 2003.

PANEL DISCUSSION

1:00pm ~ 2:00pm, Monday July 11, 2016

Ballroom B

Nanotechnology-inspired Future Computing, Challenges and Opportunities

Chair & Moderator

Prof. Yiran Chen - University of Pittsburgh

Panelists

Dr. Sankar Basu, National Science Foundation

Dr. Jonathan J. Candelaria, Semiconductor Research Corporation

Prof. Dan Hammerstrom, Portland State University

Dr. David Mountain, NSA

Prof. Vijaykrishnan Narayanan, Pennsylvania State University

Dr. Robinson Pino, Department of Energy

Dr. Qing Wu – Air Force Research Lab

Summary

In October 2015, the White House announced a Nanotechnology-Inspired Grand Challenge for Future Computing, which addresses three Administration priorities—the National Nanotechnology Initiative, the National Strategic Computing Initiative (NSCI), and the BRAIN initiative. The goal is to create a new type of computer that can proactively interpret and learn from data, solve unfamiliar problems using what it has learned, and operate with the energy efficiency of the human brain. The theme of the panel discussion is the impact of the Grand Challenge on the research of VLSI design and computing systems and how the academia and government research centers shall respond to it. Panelists from funding agencies, national laboratories, and academic institutes are invited to share their points of view and answer the questions from the conference attendants.

SESSION 01

Monday July 11, 2016

Conference Room A

Analog and Mixed Signal I

Chair: **Terry Ye, *Carnegie Mellon University***

10:00 AM **A New Process Variation Monitoring Circuit**
Davit Mirzoyan and Ararat Khachatryan

10:20 AM **Mixed-Signal Design Using Digital CAD**
Vishnu Unnikrishnan and Mark Vesterbacka

10:40 AM **An Integrated Current Mode CTLE Receiver Front End with Charge Mode Adaptation**
Divya Duvvuri and Vijaya Sankara Rao Pasupureddi

SESSION 02

Monday July 11, 2016

Gold Room

Special Session: FPGA Based Computing: Evolving Applications and Design Tools

Chair: **Tosiron Adegbija, *University of Arizona***

10:00 AM **An Automated Hardware/Software Co-Design Flow for Partially Reconfigurable FPGAs**
Shaon Yousuf and Ann Gordon-Ross

10:20 AM **Angel-Eye: A Complete Design Flow for Mapping CNN onto Customized Hardware**
Kaiyuan Guo, Lingzhi Sui, Jiantao Qiu, Song Yao, Song Han, Yu Wang and Huazhong Yang

10:40 AM **FPGA Based Cyber Security Protocol for Automated Traffic Monitoring Systems: Proposal and Implementation**
Anupam Chattopadhyay, Vikramkumar Pudi, Anubhab Baksi and Thambipillai Srikanthan

SESSION 03

Monday July 11, 2016

Conference Room A

Computer Aided Design and Verification I

Chair: **Anupam Chattopadhyay, *Nanyang Technological University***

11:00 AM **Speeding up Incremental Legalization with Fast Queries to Multidimensional Trees**
Renan Netto, Vinicius Livramento, Chrystian Guth, Luiz C. V. Dos Santos and Jose Luis Güntzel

11:20 AM **Timing Analysis and Optimization Based on Flexible Flip-Flop Timing Model**
Jeongwoo Heo and Taewhan Kim

11:40 AM **Synthesizing Asynchronous Circuits Toward Practical Use**
Heechun Park and Taewhan Kim

SESSION 04

Monday July 11, 2016

Gold Room

Special Session: Cyber-Physical Systems: Architecture and Security in Smart Buildings and Autonomous Driving

Chair: **Wujie Wen, *Florida International University***

11:00 AM **Next Generation Automotive Architecture Modeling and Exploration for Autonomous Driving**
Bowen Zheng, Hengyi Liang, Qi Zhu, Huafeng Yu and Chung-Wei Lin

11:20 AM **Online Unusual Behavior Detection for Temperature Sensor Networks**
Hengyang Zhao, Sheldon X.-D. Tan, Hai Wang, and Hai-Bao Chen

11:40 AM **Security Challenges in CPS and IoT: from End-Node to the System**
Kelvin Ly and Yier Jin

SESSION 05

Monday July 11, 2016

Conference Room A

Digital Circuit Design and FPGA Based Designs I

Chair: **Jia Di, *University of Arkansas***

2:30 PM **VLSI Architecture for Cyclostationary Feature Detection based Spectrum Sensing for Cognitive-Radio Wireless Networks and Its ASIC Implementation**
Mahesh S. Murty and Rahul Shrestha

2:50 PM **Generating Multi-Cycle and Multiple Transient Fault Resilient Design during Physically Aware High Level Synthesis**
Anirban Sengupta and Deepak Kachave

3:10 PM **Power-Performance Optimization of a Virtualized SMT Vector Processor via Thread Fusion and Lane Configuration**
Yaojie Lu, SeyedAmin Rooholamin, and Sotirios G. Ziavras

SESSION 06

Monday July 11, 2016

Gold Room

Special Session: From Neural Science to Neuromorphic Computing

Chair: **Minjie Lin, *University of Central Florida***

2:30 PM **Neuromorphic Computing from the Computer Science Perspective**
Catherine D. Schuman

2:50 PM **A VLSI Design for Neuromorphic Computing**
Mark E. Dean and Christopher Daffron

3:10 PM **Reducing the Model Order of Deep Neural Networks Using Information Theory**
Ming Tu, Visar Berisha, Yu Cao, and Jae-Sun Seo

SESSION 07

Monday July 11, 2016

Conference Room A

Emerging and Post-CMOS Technologies I

Chair: **Kamalika Datta, *NIT Meghalaya***

3:30 PM **A Reconfigurable Array Architecture for NML**
G. Causapruno, U. Garlando, F. Cairo, M. Zamboni, and M. Graziano

3:50 PM **Design and Analysis of Novel InSb/Si Heterojunction Double Gate Tunnel Field Effect Transistor**
S. Ahish, Dheeraj Sharma, M. H. Vasantha, and Y. B. N. Kumar

4:10 PM **A Memristor Crossbar Based Computing Engine Design Optimized for High Speed and Accuracy**
Chenchen Liu, Qing Yang, Bonan Yan, Jianlei Yang, Xiaocong Du, Weijie Zhu, Hao Jiang, Qing Wu, Mark Barnell and Hai Li

SESSION 08

Gold Room

Monday July 11, 2016

Special Session: Emerging Stochastic Computing: From Arithmetic to Applications

Chair: **Yanzhi Wang, *Syracuse University***

3:30 PM **Design of Division Circuits for Stochastic Computing**
Te-Hsuan Chen and John P. Hayes

3:50 PM **Adaptive Filter Design using Stochastic Circuits**
Honglan Jiang, Chengkun Shen, Pieter Jonker, Fabrizio Lombardi and Jie Han

4:10 PM **High-Accuracy FIR Filter Design using Stochastic Computing**
Bo Yuan and Yanzhi Wang

SESSION 09

Monday July 11, 2016

Conference Room A

System Design and Security I

Chair: **Jürgen Becker, *Karlsruhe Institute of Technology KIT***

4:45 PM **Design and Characterization of the TERO-PUF on SRAM FPGAs**
Cédric Marchand, Lilian Bossuet and Abdelkarim Cherkaoui

5:05 PM **Hardware/Software Isolation and Protection Architecture for Transparent Security Enforcement in Networked Devices** *Festus Hategekimana, Pierre Nardin and Christophe Bobda*

5:25 PM **A Gracefully Degrading and Energy-Efficient Fault Tolerant NoC Using Spare Core**
B. Naresh Kumar Reddy, M. H. Vasantha, and Y. B. Nithin Kumar

SESSION 10

Monday July 11, 2016

Gold Room

Testing, Reliability, and Fault-Tolerance I

Chair: **Jie Han, *University of Alberta***

4:45 PM **Analyzing Imprecise Adders Using BDDs — A Case Study** *Cunxi Yu and Maciej Ciesielski*

5:05 PM **Post-Placement Optimization for Thermal-induced Mechanical Stress Reduction** *Tiantao Lu, Zhiyuan Yang and Ankur Srivastava*

5:25 PM **Impact of VT and Body-Biasing on Resistive short detection in 28nm UTBB FDSOI – LVT and RVT configurations** *Amit Karel, Mariane Comte, Jean-Marc Galliere, Florence Azais, and Michel Renovell*

SESSION 11

Tuesday July 12, 2016

Conference Room A

Digital Circuit Design and FPGA Based Designs II

Chair: **Rahul Shrestha, *International Institute of Information Technology Hyderabad (IIIT-H)***

10:00 AM **Low Cost VLSI Architecture for Sample Adaptive Offset Encoder in HEVC** *Sayed El Gendy, Ahmed Shalaby, and Mohammed S. Sayed*

10:20 AM **Dynamic Per-warp Reconvergence Stack for Efficient Control Flow Handling in GPUs** *Yaohua Wang, Xiaowen Chen, Dong Wang, and Sheng Liu*

10:40 AM **Subthreshold Passive RFID Tag's Baseband Processor Core Design with Custom Modules and Cells** *Weiwei Shi, Zhao Guangdong, and Chiu-Sing Choy*

SESSION 12

Tuesday July 12, 2016

Gold Room

Special Session: Emerging Devices for Hardware Security: Fiction or Future

Chair: **Xiang Chen, *George Mason University***

10:00 AM **Selective Enhancement of Randomness at the Materials Level: Poly-Si Based Physical Unclonable Functions (PUFs)** *Hao-Ting Shen, Fahim Rahman, Bicky Shakya, Mark Tehranipoor, and Domenic Forte*

10:20 AM **A Designer's Rationale for Nanoelectronic Hardware Security Primitives** *Garrett S. Rose, Mesbah Uddin, and Md. Badruddoja Majumder*

10:40 AM **Hardware Security Challenges Beyond CMOS: Attacks and Remedies** *Kaveh Shamsi, Wujie Wen, and Yier Jin*

SESSION 13

Tuesday July 12, 2016

Conference Room A

System Design and Security II

Chair: **Prasun Ghosal, *IIEST, Shibpur***

11:00 AM **Attacking an SRAM-based PUF through Wearout**
Alec Roelke and Mircea R. Stan

11:20 AM **Techniques for Improved Reliability in Memristive Crossbar PUF Circuits**
Mesbah Uddin, Md. Badruddoja Majumder, Garrett S. Rose, Karsten Beckmann, Harika Manem, Zahiruddin Alamgir, and Nathaniel C. Cady

11:40 AM **LLPA: Logic state based Leakage Power Analysis**
Siva Nishok Dhanuskodi, Shahrzad Keshavarz and Daniel Holcomb

SESSION 14

Tuesday July 12, 2016

Gold Room

Special Session: The Smart-Everything Era

Chair: **Theocharis Theocharides, *University of Cyprus***

11:00 AM **Hardware Design Automation of Convolutional Neural Networks**
Andrea Solazzo, Emanuele Del Sozzo, Irene De Rose, Matteo De Silvestri, Gianluca C. Durelli, and Marco D. Santambrogio

11:20 AM **Low-Power Wearable System for Real-Time Screening of Obstructive Sleep Apnea**
Grégoire Surrel, Francisco Rincón, Srinivasan Murali and David Atienza

11:40 AM **YodaNN: An Ultra-Low Power Convolutional Neural Network Accelerator Based on Binary Weights**
Renzo Andri, Lukas Cavigelli, Davide Rossi and Luca Benini

SESSION 15

Tuesday July 12, 2016

Conference Room A

System Design and Security III

Chair: **Jürgen Becker, *Karlsruhe Institute of Technology KIT***

2:15 PM **Workload-aware Power Gating Design and Run-time Management for Massively Parallel GPGPUs**
Kapil Dev, Sherief Reda, Indrani Paul, Wei Huang and Wayne Burleson

2:35 PM **Write Pulse Scaling for Energy Efficient STT-MRAM**
Yousra Alkabani, Zach Koopmans, Haifeng Xu, Alex K. Jones, and Rami Melhem

2:55 PM **Hardware Trust through Layout Filling: a Hardware Trojan Prevention Technique**
Papa-Sidy Ba, Sophie Dupuis, Manikandan Palanichamy, Marie-Lise Flottes, Giorgio Di Natale and Bruno Rouzeyre

SESSION 16

Tuesday July 12, 2016

Gold Room

Emerging and Post-CMOS Technologies II

Chair: **Prasun Ghosal, *IIEST, Shibpur***

2:15 PM **Computing in Ribosomes: Performing Boolean Logic Using mRNA-Ribosome System**
Pratima Chatterjee, Mayukh Sarkar and Prasun Ghosal

2:35 PM **Efficient Low-Density Parity-Check (LDPC) Code Decoding for Combating Asymmetric Errors in STT-RAM**
Bohua Li, Yukui Pei and Wujie Wen

2:55 PM **System Design for In-hardware STDP Learning and Spiking Based Probablistic Inference**
Khadeer Ahmed, Amar Shrestha, Yanzhi Wang and Qinru Qiu

SESSION 17

Tuesday July 12, 2016

Conference Room A

Computer Aided Design and Verification II

Chair: **Alex Jones, *University of Pittsburgh***

3:15 PM **A Hybrid Algorithm to Conservatively Check the Robustness of Circuits**
Niels Thole, Görschwin Fey, and Alberto Garcia-Ortiz

3:35 PM **Formal Verification Using Don't-Care and Vanishing Polynomials** *Cunxi Yu and Maciej Ciesielski*

3:55 PM **Routing-aware Incremental Timing-driven Placement**
Jucemar Monteiro, Nima Karimpour Darav, Guilherme Flach, Mateus Fogaça, Ricardo Reis, Andrew Kennings, Marcelo Johann and Laleh Behjat

SESSION 18

Tuesday July 12, 2016

Gold Room

Special Session: Explorations in Energy Efficient Computing from Circuits to Systems

Chair: **Himanshu Thapliyal, *University of Kentucky***

3:15 PM **Design and Performance Evaluation of Approximate Floating-Point Multipliers**
Peipei Yin, Chenghua Wang, Weiqiang Liu and Fabrizio Lombardi

3:35 PM **Energy-Efficient Design of the Secure Better Portable Graphics Compression Architecture for Trusted Image Communication in the IoT**
Umar Albalawi, Saraju P. Mohanty, and Elias Kougianos

3:55 PM **Energy-Efficient and Secure S-Box circuit using Symmetric Pass Gate Adiabatic Logic**
S. Dinesh Kumar, Himanshu Thapliyal, Azhar Mohammad, Vijay Singh and Kalyan S. Perumalla

SESSION 19

Tuesday July 12, 2016

Conference Room A

Digital Circuit Design and FPGA Based Designs II

Chair: **Wei Zhang, *Hong Kong University of Science and Technology***

4:30 PM **Scalable Integer DCT Architecture for HEVC Encoder**
Maher Abdelrasoul, Mohammed S. Sayed, and Victor Goulart

4:50 PM **An improved approach for the synthesis of Boolean functions using memristor based IMPLY and INVERSE-IMPLY gates**
F. Lalchhandama, Brojo Gopal Sapui, and Kamalika Datta

5:10 PM **Adaptive Overclocking and Error Correction Based on Dynamic Speculation Window**
Rengarajan Ragavan, Cedric Killian and Olivier Sentieys

5:30 PM **On-chip Delay Measurement Circuit for Reliability Characterization of SRAM**
Pankaj Verma, Rohit Halba, Hemant Patel and Maryam Shojaei Baghini

SESSION 20

Tuesday July 12, 2016

Gold Room

Analog and Mixed Signal II

Chair: **Terry Ye, *Carnegie Mellon University***

4:30 PM **Digital LDO with Time-Interleaved Comparators for Fast Response and Low Ripple**
Saurav Maji, Sohail Ahasan, Saurav Maji, Kaushik Roy, and Mrigank Sharad

4:50 PM **Design of Low Power 5-bit Hybrid Flash ADC**
S. M. Mayur, R. K. Siddharth, Y. B. Nithin Kumar, and M. H. Vasantha

5:10 PM **An Accurate All CMOS Temperature Sensor for IoT Applications** *Sunil Kumar Maddikatla and Srivatsava Jandhyala*

5:30 PM **Design of Low-Power High-Gain Operational Amplifier for Bio-Medical Applications**
Sanjay Singh Rajput, Ashish Singh, Ashwani K. Chandel, and Rajeevan Chandel

POSTER SESSION

5:50pm ~ 6:50pm, Tuesday July 12, 2016

Ballroom B

P1. **A Compact Set of Seeds for LFSR-Based Test Generation from a Fully-Specified Compact Test Set**
Irith Pomeranz

P2. **Low-power and High Performance Sinusoidal Clocked Dynamic Circuit Design**
Raghava Katreepalli, Hemanth Chemanchula, Themistoklis Haniotakis, and Yiorgos Tsiatouhas

P3. **Approximate Adder with Hybrid Prediction and Error Compensation Technique**
Xinghua Yang, Yue Xing, Fei Qiao, Qi Wei and Huazhong Yang

P4. **SecCheck: A Trustworthy System with Untrusted Components**

Rajshekar Kalayappan and Smruti R. Sarangi

P5. **A Multi-Accuracy-Level Approximate Memory Architecture Based on Data Significance Analysis**
Yuanchang Chen, Xinghua Yang, Fei Qiao, Jie Han, Qi Wei, and Huazhong Yang

P6. **On Area-Efficient Implementation of Data Delays in 7 Series Xilinx FPGAs**
Marek Parfieniuk and Sang Yoon Park

P7. **Phase-based Dynamic Instruction Window Optimization for Embedded Systems**
Tosiron Adegbija and Ann Gordon-Ross

P8. **Skybridge-3D-CMOS: A Vertically-Composed Fine-Grained 3D CMOS Integrated Circuit Technology**
Mingyu Li, Jiajun Shi, Mostafizur Rahman, Santosh Khasanvis, Sachin Bhat and Csaba Andras Moritz

P9. **Fault-tolerant FPGA with Column-based Redundancy and Power Gating Using RRAM**
Kibum Lee and S. Simon Wong

P10. **Accurate Synthesis of Arithmetic Operations with Stochastic Logic**
Ensar Vahapoğlu and Mustafa Altun

P11. **A Low-Leakage, Robust ESD Clamp with Thyristor Delay Element in 65nm CMOS Technology**
Mahdi Elghazali, Manoj Sachdev and Ajoy Opal

P12. **Mod (2P-1) Shuffle Memory-Access Instructions for FFTs on Vector SIMD DSPs**
Sheng Liu, Hanyan Chen, Jianghua Wan, and Yaohua Wang

P13. **Energy Optimization of Racetrack Memory-Based SIMON Block Cipher**
Suman Deb, Anupam Chattopadhyay and Hao Yu

P17. **Power-Delay-Area Performance Modeling and Analysis for Nano-Crossbar Arrays**
Muhammed Ceylan Morgül, Furkan Peker and Mustafa Altun

P18. **Threshold-Dependent Camouflaged Cells to Secure Circuits Against Reverse Engineering Attacks**
Maria I. Mera Collantes, Mohamed El Massad, and Siddharth Garg

P19. **On the Design of Ultra-High Density 14nm Finfet based Transistor-Level Monolithic 3D ICs**
Jiajun Shi, Deepak Nayak, Motoi Ichihashi, Srinivasa Banna and Csaba Andras Moritz

P20. **A Real-Time and Energy-Efficient Implementation of Difference-of-Gaussian with Flexible Thin-Film Transistors**
Nan Wu, Zheyu Liu, Fei Qiao, Qi Wei, Xiaojun Guo, Yuan Xie, and Huazhong Yang

P21. **A Configurable and Lightweight Timing Monitor for Fault Attack Detection**
Chinmay Deshpande, Bilgiday Yuce, Nahid Farhady Ghalaty, Dinesh Ganta, Patrick Schaumont and Leyla Nazhandali

P22. **Gate Overdrive with Split-circuit Biasing to Substitute for Body Biasing in FinFET and UTB FDSOI Circuits**
Andrew Whetzel and Mircea R. Stan

P23. **Analysis of Switching Energy and Delay for Magnetic Logic Devices**
Madhav Rao and Neha Oraon

P24. **A 90-nm CMOS Frequency Synthesizer with a Tripler for 60-GHz Wireless Communication Systems**
Po-Tsang Chen and Ching-Yuan Yang

P25. **A System-Level Exploration of Power Delivery Architectures for Near-Threshold Manycores Considering Performance Constraints**
Ioannis Stamelakos, Amin Khajeh, Ahmed Eltawil, Gianluca Palermo, Cristina Silvano, and Fadi Kurdahi

P26. **Fault-tolerant Clock Synchronization with High Precision**
Attila Kinali, Florian Huemer, and Christoph Lenzen

P27. **STA: A Highly Scalable Low Latency Butterfly Fat Tree Based 3D NoC Design**
Avik Bose, Prasun Ghosal, and Saraju P. Mohanty

P28. **Leveraging Compiler Support on VLIW processors for Efficient Power Gating**
Juan S. P. Giraldo, Luigi Carro, Stephan Wong, and Antonio C. S. Beck

P29. **MINLP based Power Optimization for Pipelined ADC**
A. Purushothaman

P30. **Voice Based User-Device Physical Unclonable Functions for Mobile Device Authentication**
Yunxi Guo and Akhilesh Tyagi

P31. **Taylor Series Based Architecture for Quadruple Precision Floating Point Division**
Manish Kumar Jaiswal and Hayden K.-H. So

P32. **An Accurate All CMOS Bandgap Reference Voltage with Integrated Temperature Sensor for IoT Applications**
Sunil Kumar Maddikatla and Srivatsava Jandhyala

P33. **Thermal-aware Preemptive Test Scheduling for Network-on-Chip based 3D ICs**
Kanchan Manna, Chatla Swamy Sagar, Santanu Chattopadhyay, and Indranil Sengupta

P34. **Design Optimization of Register File Throughput and Energy using a Virtual Prototyping (ViPro) Tool**
Ningxi Liu and Benton Calhoun

P35. **A Learning-based Approach to Secure JTAG against Unseen Scan-based Attacks**
Xuanle Ren, R. D. (Shawn) Blanton, and Vítor Grade Tavares

P36. **Using Statistical Models to Improve the Reliability of Delay-Based PUFs**
Xiaolin Xu, Wayne Burleson, and Daniel E. Holcomb

P37. **Fast Multi-Level Test Generation at the RTL**
Kelson Gent and Michael S. Hsiao

P38. **Architecture Exploration for Energy-Efficient Embedded Vision Applications: From General Purpose Processor to Domain Specific Accelerator**
Maria Malik, Farnoud Farahmand, Paul Otto, Nima Akhlaghi, Tinoosh Mohsenin, Siddhartha Sikdar, and Houman Homayoun

P39. **DSD: A Dynamic State-Deflection Method for Gate-Level Netlist Obfuscation**
Jaya Dofe, Yuejun Zhang and Qiaoyan Yu

P40. **Soft Error Effect Tolerant Temporal Self-Voting Checkers: Energy vs. Resilience Tradeoffs**
Faris S. Alghareb, Mingjie Lin, and Ronald F. DeMara

P41. **Accurus: A Fast Convergence Technique for Accuracy Configurable Approximate Adder Circuits**
Vinamra Benara and Suresh Purini

STUDENT RESEARCH FORUM

5:50pm ~ 6:50pm, Tuesday July 12, 2016

Ballroom B

F1. **Thermal-Aware Design and Test Techniques for Two-and Three-Dimensional Networks-on-Chip**
Kanchan Manna, Santanu Chattopadhyay, and Indranil Sengupta

F2. **A Low-Cost Mixed Clock Generator for High Speed Adiabatic Logic**
Zhou Zhao, Ashok Srivastava, Lu Peng, and Saraju P. Mohanty

F3. **Accelerating Particle Filter on FPGA**
B. G. Sileshi, J. Oliver, and C. Ferrer

F4. **Soft-Error Tolerant Datapath Synthesis Considering Adjacency Constraint between Components**
Junghoon Oh and Mineo Kaneko

SESSION 21

Wednesday July 13, 2016

Conference Room A

System Design and Security IV

Chair: **Aymen Touati, *LIRMM CNRS***

10:00 AM **Gossip NoC - Avoiding Timing Side-Channel Attacks through Traffic Management**
Cezar Reinbrecht, Altamiro Susin, Lilian Bossuet, and Johanna Sepúlveda

10:20 AM **Leakage Power Aware Task Assignment Algorithms for Multicore Platforms**
Gayathri Ananthanarayanan, Smruti R. Sarangi and M. Balakrishnan

10:40 AM **A Design Space Exploration Methodology for Parameter Optimization in Multicore Processors**
Prasanna Kansakar and Arslan Munir

SESSION 22

Wednesday July 13, 2016

Gold Room

Special Session: Technology-aware Mapping of Algorithm to Architecture for Power, Performance, and Reliability

Chair: **Anupam Chattopadhyay, *Nanyang Technological University***

10:00 AM **Reliable Many-Core System-on-Chip Design using K-Node Fault Tolerant Graphs**
Zheng Wang, Alessandro Littarru, Emmanuel Ikechukwu Ugwu, Shazia Kanwal and Anupam Chattopadhyay

10:20 AM **Seamlessly Pipelined Shift-and-Add Circuits Based on Precise Delay Analysis and Its Applications**
Tso-Bing Juang and Ying-Ren Lee

10:40 AM **On Time Redundancy of Fault Tolerant C-Based MPSoCs**
Anjana Balachandran, Nandeesh Veeranna and Benjamin Carrion Schafer

SESSION 23

Wednesday July 13, 2016

Conference Room A

Emerging and Post-CMOS Technologies III

Chair: **Yiran Chen, *University of Pittsburgh***

11:00 AM **Cost and Thermal Analysis of High-Performance 2.5D and 3D Integrated Circuit Design Space**
Dylan Stow, Itir Akgun, Russell Barnes, Peng Gu and Yuan Xie

11:20 AM **Memristor-Based Discrete Fourier Transform for Improving Performance and Energy Efficiency**
Ruizhe Cai, Ao Ren, Yanzhi Wang and Bo Yuan

11:40 AM **Device Circuit Co Design of FEFET Based Logic for Low Voltage Processors**
Sumitha George, Ahmedullah Aziz, Xueqing Li, Moon Seok Kim, Suman Datta, John Sampson, Sumeet Gupta, and Vijaykrishnan Narayanan

SESSION 24

Wednesday July 13, 2016

Gold Room

Special Session: Scalable Design Approach

Chair: **Tosiron Adegbija, *University of Arizona***

11:00 AM **A Scalable Design Approach to Efficiently Map Applications on CGRAs**
Satyajit Das, Thomas Peyret, Kevin Martin, Gwenolé Corre, Mathieu Thevenin, and Philippe Coussy

11:20 AM **SoC, NoC and Hierarchical Bus Implementations of Applications on FPGAs Using the FCUDA Flow**
Tan Nguyen, Yao Cheny, Kyle Rupnow, Swathi Gurumani, and Deming Chen

11:40 AM **Area Efficient Hardware Architecture for Implicitly-Defined Complex Events Processing**
Mohammad Tahghighi, Wei Zhang, and Sharad Sinha

SESSION 25

Wednesday July 13, 2016

Conference Room A

Computer Aided Design and Design Methodologies

Chair: **Hai Li, *University of Pittsburgh***

1:00 PM **Design Space Exploration of FinFETs with Double Fin Heights for Standard Cell Library**
Chi-Hung Lin, Chia-Shiang Chen, Yu-He Chang, Yu-Ting Zhang, Shang-Rong Fang, Santanu Santra and Rung-Bin Lin

1:20 PM **Multiple-Bit-Flip Detection Scheme for A Soft-Error Resilient TCAM**
Infall Syafalni, Tsutomu Sasao and Xiaoqing Wen

1:40 PM **A Comparative Study of Si/Ge and GaSb/InAs Tunnel FET-based Cellular Neural Network**
Amit Ranjan Trivedi and Susmita Dey Manasi

SESSION 26

Wednesday July 13, 2016

Gold Room

Digital Circuit Design and FPGA Based Designs III

Chair: **Beiye Liu, *Amazon***

1:00 PM **A Dual-Threshold Voltage Approach for Timing Speculation in CMOS Circuits**
Xiaowen Wang and William H. Robinson

1:20 PM **Multi Clock Flooded LDPC Decoding Architecture with Reduced Memory and Interconnect**
Oana Boncalo and Ioana Mot

1:40 PM **The Impact of Heterogeneity on a Reconfigurable Multicore System**
Rafael Fão de Moura, Jeckson Dellagostin Souza, Luigi Carro, Antonio Carlos Schneider Beck, and Mateus Beck Rutzig

SESSION 27

Wednesday July 13, 2016

Conference Room A

Digital Circuit Design and FPGA Based Designs IV

Chair: **Michael Huebner, *Ruhr-Universität Bochum***

2:00 PM **A Pruning Technique for B&B based Design Exploration of Approximate Computing Variants**
Mario Barbareschi, Federico Iannucci and Antonino Mazzeo

2:20 PM **Stochastic-Based Convolutional Networks with Reconfigurable Logic Fabric**
Mohammed Alawad and Mingjie Lin

2:40 PM **A Ternary-valued, Floating Gate Transistor-based Circuit Design Approach**
Monther Abusultan and Sunil P. Khatri

SESSION 28

Wednesday July 13, 2016

Gold Room

Testing, Reliability, and Fault-Tolerance II

Chair: **Saraju Mohanty, *University of North Texas***

2:00 PM **Quantification of Sense Amplifier Offset Voltage Degradation due to Zero- and Run-time Variability**
Innocent Agbo, Mottaqiallah Taouil, Said Hamdioui, Pieter Weckx, Stefan Cosemans, Praveen Raghavan, Francky Catthoor and Wim Dehaene

2:20 PM **Improving the Functional Test Delay Fault Coverage: A Microprocessor Case Study**
A. Touati, A. Bosio, P. Girard, A. Virazel, P. Bernardi, and M. Sonza Reorda

2:40 PM **Joint Soft-Error-Rate (SER) Estimation for Combinational Logic and Sequential Elements**
Ji Li and Jeffrey Draper