ISVLSI 2017 Program Outline

Monday, July 3rd 2017	8:30 AM	-	9:30 AM	**Keynote # 1**		
	9:30 AM	-	10:00 AM	**Coffee Break**	**Coffee Break**	**Coffee Break**
	10:00 AM	-	12:00 PM	Session 01: Digital Circuits and FPGA based Designs I	Session 02: Emerging and Post-CMOS Technologies I	Session 03: System Design and Security I
	12:00 PM	-	1:00 PM	**Lunch**		
	1:00 PM	-	3:00 PM	Session 04: Digital Circuits and FPGA based Designs II	Session 05: Emerging and Post-CMOS Technologies II	Session 06: System Design and Security II
	3:00 PM	-	3:30 PM	**Coffee Break**	**Coffee Break**	**Coffee Break**
	3:30 PM	-	5:00 PM	Session 07: Digital Circuits and FPGA based Designs III	Session 08: Student Research Forum	Session 09: System Design and Security III
	6:00 PM	-	8:00 PM	**Welcome Reception**		
Tuesday, July 4th 2017	8:30 AM	-	9:30 AM	**Keynote # 2**		
	9:30 AM	-	10:00 AM	**Coffee Break**	**Coffee Break**	**Coffee Break**
	10:00 AM	-	12:00 PM	Session 10: Testing, Reliability, and Fault-Tolerance I	Session 11: Research Projects	Session 12: System Design and Security IV
	12:00 PM	-	1:00 PM	**Lunch** **ISVLSI Steering Committee Meeting**		
	1:00 PM	-	2:00 PM	**Distignuished Lecture**		
	2:00 PM	-	4:00 PM	Session 13: Testing, Reliability, and Fault-Tolerance II	Session 14: Computer-Aided Design and Verification I	Session 15: System Design and Security V
	4:00 PM	-	5:00 PM	**Poster Session**		
	6:00 PM	-	9:00 PM	**Rhine Boat Trip**		
Wednesday, July 5th 2017	8:30 AM	-	9:30 AM	**Keynote # 3**		
	9:30 AM	-	10:00 AM	**Coffee Break**	**Coffee Break**	**Coffee Break**
	10:00 AM	-	12:00 PM	Session 16: Analog and Mixed-Signal Circuits I	Session 17: Computer-Aided Design and Verification II	**Special Session 01:** Post CMOS Computing - Emerging Technologies and Design Issues
	12:00 PM	-	1:00 PM	**Lunch**		
	1:00 PM	-	3:00 PM	Session 18: Analog and Mixed-Signal Circuits II	**Special Session 02:** Emerging Computing Paradigms for Energy-Efficient and Secure IoT Devices	**Special Session 03:** Adaptive Circuits and Systems for Machine Intelligence: The role of adaptive circuits and systems in emerging intelligent systems and networks
	3:00 PM	-	3:30 PM	**Coffee Break**	**Coffee Break**	**Coffee Break**
	3:30 PM	-	5:30 PM	Session 19: Analog and Mixed-Signal Circuits III	**Special Session 04:** Emerging and Secured Applications of IoT (Internet of Things)	**Special Session 05:** Innovation in Memory Technologies and Their Applications
	5:30 PM	-	6:00 PM	**Closing Remarks and Award Ceremony**		

KEYNOTE 1

Monday, July 3rd 2017

8:30 – 9:30

Chair: Mircea Stan

Electronic circuit design for the smart world era

Prof. Georges Gielen

University of Leuven

Summary

The relentless progress of nanoelectronics and semiconductor technology fuel the technological revolution towards a smart world that immersively impacts our daily life, work and play. Proactive healtcare monitoring, wellbeing comforting, cloud-based services, autonomous driving, industry 4.0, etc. are but a few examples. After introducing the broader context, this keynote will focus on core challenges and possible solution paths to the design of electronic circuits for these emerging applications. Design techniques and circuit solutions will be presented towards high energy efficiency, low cost and high robustness. This will be illustrated with some practical IC design examples for sensor-based applications.

KEYNOTE 2

Tuesday, July 4th 2017

8:30 – 9:30

Chair: Michael Hübner

History and Future of Megatrends in EDA industry

Mr Jens C. Werner

Vice President, Cadence, Field Engineering EMEA

Speaker Bio

Mr. Werner joined Cadence in 1992 as an Application Engineer in Munich. His career with Cadence has spanned 25 years where he has held a variety of engineering and leadership roles in Field Engineering and Services. In 2010,he was appointed leader of the Technical Field Engineering team in EMEA. Prior to his current position, Mr. Werner co-led the VCAD services team in EMEA, built up the Services presence in the Asia Pacific region and headed the global Services Business Program Management team. Mr. is instrumental in driving the development of new capabilities in the Field Engineering team EMEA and has established a program to strengthen the team by hiring experienced industry talent as well as recent graduates. He is customer focused and firmly believes the customer should always be the number one priority.

Mr. Werner has over 25 years of experience in electronics and engineering. His areas of expertise include leadership, problem solving, semiconductors, integrated circuits and systems. Prior to joining Cadence Design Systems, Mr. Werner worked as a design engineer for Nanotron Technologies. Attributing his success to his leadership abilities together with his in-depth knowledge of the electronics industry, Mr. Werner enjoys working with productive and innovative teams. He became involved in his profession due to studying Microelectronics in college and was attracted to the fast-paced nature of the industry. Mr. Werner received a Master's degree in Microelectronics from the Technical University of Berlin. He is also affiliated with ACM and IEEE. Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software, hardware, IP, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry.

DISTINGUISHED LECTURE

Tuesday, July 4th 2017

13:00 – 14:00

Chair: Ricardo Reis

Pushing the Limits of Technology, Circuit and Applications for Sub-nm Low Power Design

Dr. Rajiv Joshi

Summary

Power has become the key driving force in processor design as the frequency scale-up is reaching saturation. In order to achieve low power system circuit and technology co-design is essential. This talk focuses on related technology and important circuit techniques for nanoscale VLSI circuits. Achieving low power and high performance simultaneously is always difficult. Technology has seen major shifts from bulk to SOI and then to non-planar devices such as FinFET and Trigates.

This talk consists of pros and cons analysis on technology from power perspective and various techniques to exploit lower power. As the technology pushes towards sub-22nm era, process variability and geometric variation in devices can cause variation in power. The reliability also plays an important role in the power-performance envelope. This talk also reviews the methodology to capture such effects and describes all the power components. All the key areas of low power optimization such as reduction in active power, leakage power, short circuit power and collision power are covered. Usage of clock gating, power gating, longer channel, multi-Vt design, stacking, header-footer device techniques and other innovative methods are described for logic and memory. Low power memories are essential part of neural networks and the talk will describe some of these memories slated for machine learning. Finally the talk summarizes key challenges in achieving low power.

Speaker Bio

Dr. Rajiv V. Joshi is a research staff member and key technical lead at T. J. Watson research center, IBM. He received his B.Tech I.I.T (Bombay, India), M.S (M.I.T) and Dr. Eng. Sc.

(Columbia University). His novel interconnects processes and structures for aluminum, tungsten and copper technologies which are widely used in IBM for various technologies from sub-0.5µm to 14nm. He has led successfully predictive failure analytic techniques for yield prediction and also the technology-driven SRAM at IBM Server Group. He commercialized these techniques. He received 3 Outstanding Technical Achievement (OTAs), 3 highest Corporate Patent Portfolio awards for licensing contributions, holds 58 invention plateaus and has over 225 US patents and over 350 including international patents. He has authored and co-authored over 185 papers. He received the Best Editor Award from IEEE TVLSI journal. He is recipient of 2015 BMM award. He is inducted into New Jersey Inventor Hall of Fame in Aug 2014 along with pioneer Nikola Tesla. He is a recipient of 2013 IEEE CAS Industrial Pioneer award and 2013 Mehboob Khan Award from Semiconductor Research Corporation. He is a member of IBM Academy of technology. He served as a Distinguished Lecturer for IEEE CAS and EDS society. He is IEEE, ISQED and World Technology Network fellow and distinguished alumnus of IIT Bombay. He is in the Board of Governors for IEEE CAS. He serves as an Associate Editor of TVLSI. He served on committees of ISLPED (Int. Symposium Low Power Electronic Design), IEEE VLSI design, IEEE CICC, IEEE Int. SOI conference, ISQED and Advanced Metallization Program committees. He served as a general chair for IEEE ISLPED. He is an industry liaison for universities as a part of the Semiconductor Research Corporation. Also he is in the industry liaison committee for IEEE CAS society.

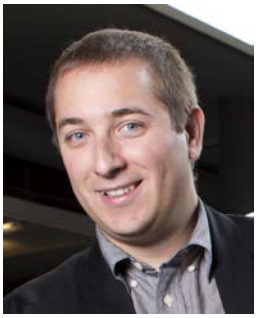
KEYNOTE 3

Wednesday, July 5th 2017

8:30 – 9:30

Chair: Nikolaos Voros

What About Increasing the Functionality of Devices Rather Than Scaling Them?



Pierre-Emmanuel Gaillardon, PhD

University of Utah

Summary

Exploiting unconventional physical properties, several nanodevices showed an alternative to Moore's Law by the increase of their functionality rather than the pure scaling. Innovative device behaviors transduce to new circuit/architecture opportunities. Here, we will introduce Three-Independent-Gate Field Effect Transistors (TIGFETs), a novel class of computation devices, that can, depending on the bias applied to its gate, achieve different modes of operations usually not achievable in a single device. The demonstrated modes of operations are (i) the dynamic reconfiguration of the device polarity; (ii) the dynamic control of the threshold voltage; and (iii) the dynamic control of the subthreshold slope beyond the thermal limit (with a measured steep slope of 6mV/dec over 5 decades of current). I will show both a silicon-based process route and a 2D approach based on WSe2 crystals. Such properties are highly desirable for logic computation. For instance, controllable-polarity devices are logical bi-conditional on both gate values and enable a compact realization of XOR-based logic functions, which are not implementable in CMOS in a compact form. Hyper regular architectures and new EDA tools are then needed to leverage the intrinsic properties of controllable-polarity devices from an application perspective. In this talk, I will cover the different aspects of the design with TIG devices ranging from device fabrication to logic synthesis tools, emphasizing on the importance for interdisciplinary teams in the field of emerging technologies.

Speaker Bio

Pierre-Emmanuel Gaillardon is an assistant professor in the Electrical and Computer Engineering (ECE) department at The University of Utah, Salt Lake City, UT and he leads the Laboratory for

NanoIntegrated Systems (LNIS). He holds an Electrical Engineer degree from CPE-Lyon, France (2008), a M.Sc. degree in Electrical Engineering from INSA Lyon, France (2008) and a Ph.D. degree in Electrical Engineering from CEA-LETI, Grenoble, France and the University of Lyon, France (2011). Prior to joining the University of Utah, he was a research associate at the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland within the Laboratory of Integrated Systems (Prof. De Micheli) and a visiting research associate at Stanford University, Palo Alto, CA, USA. Previously, he was research assistant at CEA-LETI, Grenoble, France. Prof. Gaillardon is recipient of the C-Innov 2011 best thesis award and the Nanoarch 2012 best paper award. He is an Associate Editor of the IEEE Transactions on Nanotechnology. He has been serving as TPC member for many conferences, including DATE'15-16, DAC'16, Nanoarch'12-16, and is reviewer for several journals and funding agencies. He will serve as Topic co-chair “Emerging Technologies for Future Memories” for DATE'17. The research activities and interests of Prof. Gaillardon are currently focused on the development of reconfigurable logic architectures and digital circuits exploiting emerging device technologies and novel EDA techniques.

SESSION 01

Monday July 3rd, 2017

Digital Circuits and FPGA based Designs I

10:00-12:00

Chair: **Djones Lettnin**

10:00 – 10:20	**Voltage Noise Analysis with Ring Oscillator Clocks** *Lucas Machado, Antoni Roca and Jordi Cortadella*	**Full Paper**
10:20 – 10:40	**Resilient Cell-Based Architecture for Time-to-Digital Converter** *Chia-Hua Wu, Shi-Yu Huang, Mason Chern, Yung-Fa Chou and Ding-Ming Kwai*	**Full Paper**
10:40 – 11:00	**Reconfigurable Support Vector Machine Classifier with Approximate Computing** *Martin van Leussen, Jos Huisken, Lei Wang, Hailong Jiao and José Pineda de Gyvez*	**Full Paper**
11:00 – 11:20	**Unconventional Layout Techniques for a High Performance, Low Variability Subthreshold Standard Cell Library** *Jordan Morris, Pranay Prabhat, James Myers and Alex Yakovlev*	**Full Paper**
11:20 – 11:35	**SiLago-CoG: Coarse-grained Grid-based design for near tape-out power estimation accuracy at high level** *Syed Mohammad Asad Hassan Jafri, Nasim Farahini and Ahmed Hemani*	**Short Paper**
11:35 – 11:45	**High Speed Power Efficient Carry Select Adder Design** *Raghava Katreepalli and Themistoklis Haniotakis*	**Short Paper**

SESSION 02

Monday July 3rd, 2017

Emerging and Post-CMOS Technologies I

10:00-12:00

Chair: **Hassan Mostafa**

10:00 – 10:25	**Architecting SOT-RAM Based GPU Register File** *Sparsh Mittal, Rajendra Bishnoi, Fabian Oboril, Haonan Wang, Mehdi Tahoori, Adwait Jog and Jeffrey Vetter*	**Full Paper**
10:25 – 10:50	**RIMPA: A New Reconfigurable Dual-Mode In-Memory Processing Architecture with Spin Hall Effect-Driven Domain Wall Motion Device** *Shaahin Angizi, Zhezhi He, Farhana Parveen and Deliang Fan*	**Full Paper**
10:50 – 11:15	**Area and Delay Efficient Design of a Quantum Bit String Comparator** *Hafiz Md Hasan Babu, Lafifa Jamal, Sayanton Vhaduri Dibbo and Ashis Kumer Biswas*	**Full Paper**
11:15 – 11:30	**Novel Pulsed-Latch Replacement in Non-Volatile Flip-Flop Core** *Hao Cai, You Wang, Lirida Naviner and Weisheng Zhao*	**Short Paper**
11:30 – 11:45	**Analysis of RRAM Reliability Soft-Errors on the Performance of RRAM-based Neuromorphic Systems** *Amr Tosson, Shimeng Yu, Mohab Anis and Lan Wei*	**Short Paper**
11:45– 12:00	**Design of Quantum Circuits for Galois Field Squaring and Exponentiation** *Edgard Munoz-Coreas and Himanshu Thapliyal*	**Short Paper**

SESSION 03

Monday July 3rd, 2017

System Design and Security I

10:00-12:00

Chair: **Avesta Sasan**

10:00 – 10:25	**STBC: Side Channel Attack Tolerant Balanced Circuit with Reduced Propagation Delay** *Hyunmin Kim, Seokhie Hong, Bart Preneel and Ingrid Verbauwhede*	**Full Paper**
10:25 – 10:50	**AICNN: Implementing Typical CNN Algorithms with Analog-to-Information Conversion Architecture**	**Full Paper**

	Kaige Jia, Zheyu Liu, Fei Qiao, Xingjun Liu, Wei Qi and Huazhong Yang	
10:50 – 11:15	**Efficient FPGA Implementation of the SHA-3 Hash Function** *Magnus Sundal and Ricardo Chaves*	**Full Paper**
11:15 – 11:30	**Decoupling Translation Lookaside Buffer Coherence from Cache Coherence** *Hao Liu, Quentin Meunier and Alain Greiner*	**Short Paper**
11:30 – 11:45	**Centrality Indicators For Efficient And Scalable Logic Masking** *Brice Colombier, Lilian Bossuet and David Hely*	**Short Paper**
11:45– 12:00	**Combined TDM and SDM Circuit Switching NoCs with Dedicated Connection Allocator** *Yong Chen, Emil Matus and Gerhard Fettweis*	**Short Paper**

SESSION 04

Monday July 3rd, 2017

Digital Circuits and FPGA based Designs II

13:00-15:00

Chair: **Jia Di**

13:00 – 13:20	**Efficient Single Precision Floating-Point Division Using Harmonized Parabolic Synthesis** *Suleyman Savas, Erik Hertz, Tomas Nordström and Zain Ul-Abdin*	**Full Paper**
13:20 – 13:40	**An Efficient Design of an FPGA-Based Multiplier using LUT Merging Theorem** *Zarrin Tasnim Sworna, Mubin Ul Haque, Hafiz Md. Hasan Babu, Lafifa Jamal and Asish Kumer Biswas*	**Full Paper**
13:40 – 14:00	**High-performance and energy-efficient 256-bit CMOS Priority Encoder** *Dimitrios Balobas and Nikos Konofaos*	**Full Paper**
14:00 – 14:20	**Improving FPGA Design With Monolithic 3D Integration using High Dense Inter-Stack Via** *Srivatsa Rangachar Srinivasa, Karthik Mohan, Wei-Hao Chen, Kuo-Hsinag Hsu, Xueqing Li, Meng-Fan Chang, Sumeet Kumar Gupta, John Sampson and Vijaykrishnan Narayanan*	**Full Paper**
14:20 – 14:45	**Floating-Point Arithmetic using GPGPU on FPGAs**	**Full Paper**

	Muhammed Al Kadi, Benedikt Janßen and Michael Huebner	
14:45 – 15:00	**Minimizing Critical Access Time for 3D Data Bus Based on Inserted Bus Switches and Repeaters** *Chia-Chun Tsai*	**Short Paper**

SESSION 05

Monday July 3rd, 2017

Emerging and Post-CMOS Technologies II

13:00-15:00

Chair: **Hailong Jiao**

13:00 – 13:25	**Sample Preparation on Micro-Electrode-Dot-Array Digital Microfluidic Biochips** *Zipeng Li, Kelvin Yi-Tse Lai, Krishnendu Chakrabarty, Tsung-Yi Ho and Chen-Yi Lee*	**Full Paper**
13:25 – 13:50	**Hybrid Polymorphic Logic Gate with 5-Terminal Magnetic Domain Wall Motion Device** *Farhana Parveen, Zhezhi He, Shaahin Angizi and Deliang Fan*	**Full Paper**
13:50 – 14:15	**Ultra-Low Energy Data Driven Computing Using Asynchronous Micropipelines and Nano-Electro-Mechanical Relays** Haider Alrudainy, Andrey Mokhov, Fei Xia and Alex Yakovlev	**Full Paper**
14:15 – 14:30	**Inverter Propagation and Fan-out Constraints for Beyond-CMOS Majority-based Technologies** *Eleonora Testa, Odysseas Zografos, Mathias Soeken, Adrien Vaysset, Mauricio Manfrini, Rudy Lauwereins and Giovanni De Micheli*	**Short Paper**
14:30 – 14:45	**BioViz: An Interactive Visualization Engine for the Design of Digital Microfluidic Biochips** *Jannis Stoppe, Oliver Keszocze, Maximilian Luenert, Robert Wille and Rolf Drechsler*	**Short Paper**
14:45 – 15:00	**Scouting Logic: A Novel Memristor-Based Logic Design for Emerging Resistive Computing** *Lei Xie, Hoang Anh Du Nguyen, Jintao Yu, Ali Kaichouhi, Mottaqiallah Taouil and Said Hamdioui*	**Short Paper**

SESSION 06

Monday July 3rd, 2017

System Design and Security II

13:00-15:00

Chair: **Georgios Keramidas**

13:00 – 13:25	**Latency Aware Block Replacement for L1 Caches in Chip MultiProcessors** *Shirshendu Das and Hemangee K. Kapoor*	**Full Paper**
13:25 – 13:50	**Wireless NoCs using Directional and Substrate Propagation Antennas** *Vasil Pano, Yuqiao Liu, Isikcan Yilmaz, Ankit More, Baris Taskin and Kapil Dandekar*	**Full Paper**
13:50 – 14:15	**A Multi-Gbps Fully Pipelined Layered Decoder for IEEE 802.11n/ac/ax LDPC Codes** *Saleh Usman, Mohammad M. Mansour and Ali Chehab*	**Full Paper**
14:15 – 14:30	**A Meta-Routing Method to Create Multiple Virtual Logical Networks on a Single Hardware NoC** *Hela Belhadj Amor, Hamed Sheibanyrad and Frédéric Petrot*	**Short Paper**
14:30 – 14:45	**Secured-by-Design FPGA against Early Evaluation** *Ziyad Almohaimeed and Mihai Sima*	**Short Paper**
14:45 – 15:00	**Customizing Skewed Trees for Fast Memory Integrity Verification in Embedded Systems** Saru Vig, Tan Yng Tzer, Guiyuan Jiang and Siew Kei Lam	**Short Paper**

SESSION 07

Monday July 3rd, 2017

Digital Circuits and FPGA based Designs III

15:30-17:00

Chair: **Djones Lettnin**

15:30 – 15:50	**A New High Performance VLSI Architecture for LMS Adaptive Filter using Distributed**	**Full Paper**

	Arithmetic *Mohd Khan and Shaik Ahamed*	
15:50 – 16:10	**Ultra High Throughput Unrolled Layered Architecture for QC-LDPC Decoders** *Oana Boncalo and Alexandru Amaricai*	**Full Paper**
16:10 – 16:30	**A General Design Framework for Sparse Parallel Prefix Adders** *Soumya Banerjee and Wenjing Rao*	**Full Paper**
16:30 – 16:50	**On Benchmarking Pin Access for Nanotechnology Standard Cells** *Shang-Rong Fang, Cheng-Wei Tai and Rung-Bin Lin*	**Full Paper**
16:50 – 17:00	**A Power Efficient System Design Methodology Employing Approximate Arithmetic Units** *Tuba Ayhan, Fırat Kula and Mustafa Altun*	**Short Paper**

SESSION 08

Monday July 3rd, 2017

Student Research Forum

15:30-17:00

Chair: **Deliang Fang and Michael Hübner**

15:30 – 15:55	**A Side-channel Attack Resistant AES with 500Mbps, 1.92pJ/bit PVT Variation Tolerant True Random Number Generator** *Yimai Peng, Xun Sun, Haobo Zhao and Chen Sun*	**Full Paper**
15:55 – 16:20	**Unobtrusive Wearable Health Monitoring System** *Ali Aboughaly and Mohamed Abdel-Ghany*	**Full Paper**
16:20 – 16:35	**Low Power Image Acquisition Scheme Using On-Pixel Event Driven Halftoning** *Sangamesh Kodge, Himanshu Chaudhary and Mrigank Sharad*	**Full Paper**
16:35 – 17:00	**Low Power Implantable Spike Sorting Scheme based on Neuromorphic Classifier with Supervised Training Engine** *Rakshit Pathak, Saurabh Dash, Anand Mukhopadhyay, Arindam Basu and Mrigank Sharad*	**Full Paper**

SESSION 09

Monday July 3rd, 2017

System Design and Security III

15:30-17:00

Chair: **Nele Mentens**

15:30 – 15:55	**A Power Delivery Network and Cell Placement Aware IR-drop Mitigation Technique: Harvesting Unused Timing slacks to Schedule Useful Skews** *Lakshmi Bhamidipati, Bhoopal Gunna, Houman Homayoun and Avesta Sasan*	**Full Paper**
15:55 – 16:20	**Physical Design Variation in Relative Timed Asynchronous Circuits** *Tannu Sharma and Ken Stevens*	**Full Paper**
13:50 – 14:15	**Exploiting Bus Communication to Improve Cache Attacks on Systems-on-Chips** *Johanna Sepulveda, Mathieu Gross, Andreas Zankl and Georg Sigl*	**Full Paper**
16:20 – 16:35	**Detection of Layout-Level Trojans by Monitoring Substrate with Preexisting Built-in Sensors** *Leonel Acunha Guimarães, Rodrigo Possamai Bastos and Laurent Fesquet*	**Short Paper**
16:35 – 16:50	**Coding for Efficient Caching in Multicore Embedded Systems** *Tosiron Adegbija and Ravi Tandon*	**Short Paper**
16:50 – 17:00	**A Workload Characterization for the Internet of Medical Things (IoMT)** *Ankur Limaye and Tosiron Adegbija*	**Short Paper**

SESSION 10

Tuesday, July 4th 2017

Testing, Reliability, and Fault-Tolerance I

10:00-12:00

Chair: **Garrett Rose**

10:00 – 10:25	**Functional Broadside Test Generation Using a Commercial ATPG Tool**	**Full Paper**

	Naixing Wang, Bo Yao, Xijiang Lin and Irith Pomeranz	
10:25 – 10:50	**Static Compaction by Merging of Seeds for LFSR-Based Test Generation** *Irith Pomeranz*	**Full Paper**
10:50 – 11:15	**Comprehensive Study for Detection of Weak Resistive Open and Short Defects in FDSOI Technology** *Amit Karel, Florence Azais, Mariane Comte, Jean-Marc Galliere, Michel Renovell and Keshav Singh*	**Full Paper**
11:15 – 11:30	**Offset Analysis and Design Optimization of a Dynamic Sense Amplifier for Resistive Memories** *Salmen Mraihi, Elmehdi Boujamaa, Cyrille Dray and Jacques-Olivier Klein*	**Short Paper**
11:30 – 11:45	**Efficient Metastability-Containing Multiplexers** *Stephan Friedrichs and Attila Kinali*	**Short Paper**
11:45– 12:00	**Micro Latch-up Analysis on Ultra-Nanometer VLSI Technologies: A new Monte Carlo Approach** *Sarah Azimi and Luca Sterpone*	**Short Paper**

SESSION 11

Tuesday, July 4th 2017

Research Projects

10:00-12:00

Chair: **Tannu Sharma**

10:00 – 10:20	**GREAT: heteroGeneous integRated magnetic tEchnology using multifunctional standardized sTack** *Mehdi Tahoori, Sarath Mohanachandran Nair, Rajendra Bishnoi, Sophiane Senni, Jad Mohdad, Frederick Mailly, Lionel Torres, Pascal Benoit, Pascal Nouet, Rui Ma, Martin Kreißig, Frank Ellinger, Kotb Jabeur, Pierre Vanhauwaert, Gregory Di Pendina, and Guillaume Prenat*	**Full Paper**
10:20 – 10:40	**Project HIPNOS: Case Study of High Performance Avionics for Active Debris Removal in Space** *George Lentaris, Ioannis Stratakos, Ioannis Stamoulias, Konstantinos Maragos, Dimitrios*	**Full Paper**

	Soudris, Manolis Lourakis, Xenophon Zabulis and David Gonzalez-Arjona	
10:40 – 11:00	**Hardware Security for Critical Infrastructures - CIPSEC project approach** *Apostolos Fournaris, Konstantinos Lampropoulos and Odysseas Koufopavlou*	**Full Paper**
11:00 – 11:20	**AEGLE's Cloud Infrastructure for Resource Monitoring and Containerized Accelerated Analytics** *Konstantina Koliogeorgi, Dimosthenis Masouros, Georgios Zervakis, Sotirios Xydis, Tobias Becker, Georgi Gaydadjiev and Dimitrios Soudris*	**Full Paper**
11:20 – 11:40	**A CAD Open Platform for high performance reconfigurable systems in the EXTRA project** *Marco Rabozzi, Rolando Brondolin, Giuseppe Natale, Emanuele Del Sozzo, Michael Huebner, Andreas Brokalakis, Catalin Ciobanu, Dirk Stroobandt and Marco D. Santambrogio*	**Full Paper**
11:40 – 12:00	**Profile-driven Power Optimizations for AAL Robots: Maximizing Robots Idle Time by Offloading Monitoring Workload to Dedicated Hardware Components** *Georgios Keramidas, Nikolaos Voros, Christos Antonopoulos, Fynn Schwiegelshohn, Philipp Wehner, Diana Göhringer , Evaggelinos Mariatos*	**Full Paper**

SESSION 12

Tuesday, July 4th 2017

System Design and Security IV

10:00-12:00

Chair: **Hai Zhou**

10:00 – 10:25	**Unified Model for Contrast Enhancement and Denoising** *Alex Pappachen James, Olga Krestinskaya and Joshin John Mathew*	**Full Paper**
10:25 – 10:50	**SDN-Based Circuit-Switching for Many-Cores** *Marcelo Ruaro, Henrique Medina and Fernando Moraes*	**Full Paper**
10:50 – 11:15	**NEDA: NOP Exploitation with Dependency Awareness for Reliable VLIW Processors**	**Full Paper**

	Rafail Psiakis, Angeliki Kritikakou and Olivier Sentieys	
11:15 – 11:30	**Serial ATA Commands Logger for Security Monitoring on FPGA Devices** *Dan Cristian Turicu, Octavian Cret and Lucia Vacariu*	**Short Paper**
11:30 – 11:45	**PACT: Priority-Aware Phase-based Cache Tuning for Embedded Systems** *Sam Gianelli and Tosiron Adegbija*	**Short Paper**
11:45 – 12:00	**CAPSL: The Component Authentication Process for Sandboxed Layouts** *Taylor Whitaker and Christophe Bobda*	**Short Paper**

SESSION 13

Tuesday, July 4th 2017

Testing, Reliability, and Fault-Tolerance II

14:00-16:00

Chair: **Jim Harkin**

14:00 – 14:25	**Formal Verification of Truncated Multipliers using Algebraic Approach and Re-synthesis** *Tiankai Su, Cunxi Yu, Atif Yasin and Maciej Ciesielski*	**Full Paper**
14:25 – 14:50	**Assessing Self-repair on FPGAs with Biologically realistic Astrocyte-neuron Networks** *Shvan Karim, Jim Harkin, Liam McDaid, Bryan Gardiner, Andrew Tyrrell, Junxiu Liu, David Halliday, Jon Timmis, Alan Millard and Anju Johnson*	**Full Paper**
14:50 – 15:15	**Memristor-Based Clock Design and Optimization with In-situ Tunability** *Shuyu Kong, Jie Gu and Hai Zhou*	**Full Paper**
15:15 – 15:40	**Reconfigurable Hardened Latch and Flip-Flop for FPGAs** *Hamzeh Ahangari, Ihsen Alouani, Ozcan Ozturk and Smail Niar*	**Full Paper**

SESSION 14

Tuesday, July 4th 2017

Computer-Aided Design and Verification I

14:00-16:00

Chair: **Djones Lettnin**

14:00 – 14:25	**Efficient Reconfigurable Global Network-on-chip Designs towards Heterogeneous CPU-GPU Systems: An Application-Aware Approach** *Tung Le, Dan Zhao and Magdy Bayoumi*	**Full Paper**
14:25 – 14:50	**Parallel Simulation-Based Verification of RC Power Grids** *Mohammad Fawaz and Farid N. Najm*	**Full Paper**
14:50 – 15:15	**An Effective Power Grid Optimization Approach for the Electromigration Reliability** *Ming Yan, Yici Cai, Chenguang Wang and Qiang Zhou*	**Full Paper**
15:15 – 15:25	**On Tolerating Faults of TSV/Microbumps for Power Delivery Networks in 3D IC** *Sheng-Hsin Fang, Chang-Tzu Lin, Wei-Hsun Liao, Chien-Chia Huang, Li-Chin Chen, Hung-Ming Chen, I-Hsuan Lee, Ding-Ming Kwai and Yung-Fa Chou*	**Short Paper**
15:25 – 15:35	**WT-CTS: Incremental Delay Balancing Using Parallel Wiring Type For CTS** *Scott Lerner and Baris Taskin*	**Short Paper**
15:35 – 15:50	**Automatic Assertion Generation for Simulation, Formal Verification and Emulation** *Tong Zhang, Daniel Saab and Jacob A. Abraham*	**Short Paper**

SESSION 15

Tuesday, July 4th 2017

System Design and Security V

14:00-16:00

Chair: **Prasun Ghosal**

14:00 – 14:25	**Cache partitioning + loop tiling: A methodology for effective shared cache management** *Vasilis Kelefouras, Georgios Keramidas and Nikolaos Voros*	**Full Paper**
14:25 – 14:50	**OFDM based High Data Rate, Fading Resilient Transceiver for Wireless Networks-on-Chip**	**Full Paper**

	Sri Harsha Gade, Sakshi Garg and Sujay Deb	
14:50 – 15:15	**DENA: A DVFS-capable hEterogeneous NoC Architecture** *Luca Cremona, William Fornaciari, Andrea Marchese, Michele Zanella and Davide Zoni*	**Full Paper**
15:15 – 15:40	**Exploiting Configurability as a Defense Against Cache Side Channel Attacks** *Chenxi Dai and Tosiron Adegbija*	**Full Paper**

SESSION 16

Wednesday, July 5th 2017

Analog and Mixed-Signal Circuits I

10:00-12:00

Chair: **Andrés Amaya**

10:00 – 10:25	**CCATDC: A Configurable Compact Algorithmic Time-to-Digital Converter** *Shuo Li, Xiaolin Xu and Wayne Burleson*	**Full Paper**
10:25 – 10:50	**AIsim: Functional Simulator for Analog-to-Information Perceptual Systems** *Hong Liu, Zheyu Liu, Fei Qiao, Mark Po-Hung Lin, Wei Qi and Huazhong Yang*	**Full Paper**
10:50 – 11:15	**A Hierarchical and Programmable OTA-C Filter** *Mousumi Bhanja and Baidyanath Ray*	**Full Paper**
11:15 – 11:30	**A 0.3V Low Cost Low Power 24 GHz Low Noise Amplifier with Body Bias Technology** *Ming-Yu Huang, Ren-Yuan Huang and Ro-Min Weng*	**Short Paper**
11:30 – 11:45	**Capacitor Mismatch Calibration Technique to Improve the SFDR of 14-bit SAR ADC** *Hua Fan, Franco Maloberti, Dagang Li, Daqian Hu, Yuanjun Cen and Hadi Heidari*	**Short Paper**
11:45 – 12:00	**Design of an Asynchronous Detector with Priority Encoding Technique** *Keunyeol Park, Ohoon Kwon, Hyunseob Noh, Minhyun Jin and Minkyu Song*	**Short Paper**

SESSION 17

Wednesday, July 5th 2017

Computer-Aided Design and Verification II

10:00-12:00

Chair: **Rajendra Bishnoi**

10:00 – 10:25	**Towards Making Fault Injection on Abstract Models a More Accurate Tool for Predicting RT-Level Effects** *Tino Flenker, Jan Malburg, Goerschwin Fey, Serhiy Avramenko, Massimo Violante and Matteo Sonza Reorda*	**Full Paper**

10:25 – 10:50	**Transistor temperature deviation analysis in monolithic 3D standard cells** *Mélanie Brocard, Benoit Mathieu, Jean-Philippe Colonna, Cristiano Lopes Dos Santos, Cao-Minh Vincent Lu, Claire Fenouillet-Beranger, Laurent Brunet, Perrine Batude, Sebastien Thuries, Gerald Cibrario, Francois Andrieu and Olivier Billoint*	**Full Paper**
10:50 – 11:15	**Reducing Search Space for Fault Diagnosis: A Probability-based Scoring Approach** *Hossein Sabaghian-Bidgoli, Payman Behnam, Bijan Alizade and Zain Navabi*	**Full Paper**
11:15 – 11:30	**Layout Vulnerability Reduction against Trojan Insertion using Security-aware White Space Distribution** *Hamed Hossein-Talaee and Ali Jahanian*	**Short Paper**
11:30 – 11:45	**Semiformal Verification of Software-controlled Connections** *Tomas Grimm, Djones Lettnin and Michael Huebner*	**Short Paper**

SPECIAL SESSION 01

Wednesday, July 5th 2017

Post CMOS Computing - Emerging Technologies and Design Issues

10:00-12:00

Chairs:

Prasun Ghosal, Indian Institute of Engineering Science and Technology,Shibpur, India

Kamalakanta Mahapatra, National Institute of Technology, Rourkela, India

10:00 – 10:25	**Compact Modeling of Graphene Barristor for Digital Integrated Circuit Design** *Zhou Zhao, Xinlu Chen, Ashok Srivastava, Lu Peng, Saraju P. Mohanty,*	**Full Paper**
10:25 – 10:50	**Performing Mathematics using DNA: Complex Number Arithmetic using Sticker Model** *Mayukh Sarkar, Prasun Ghosal*	**Full Paper**
10:50 – 11:15	**Analysis of Side-Channel Attack AES Hardware Trojan Benchmarks against Countermeasures** *Sudeendra Kumar K, Sauvagya Sahoo, Abhishek Mahapatra, Ayas Kanta Swain, K.K.Mahapatra*	**Full Paper**

SESSION 18

Wednesday, July 5th 2017

Analog and Mixed-Signal Circuits II

13:00-15:00

Chair: **Xingyuan TONG**

13:00 – 13:25	**A VCO-Based MPPT Circuit for Low-Voltage Energy Harvesters** *Ali Hassan, Esraa Hamed, Eman Badr, Omar Sharkawy, Hassan Mostafa and Yehea Ismail*	**Full Paper**
13:25 – 13:50	**Design of 5-bit Flash ADC using Multiple Input Standard Cell Gates for Large Input Swing** *Sumit Khalapure, Siddharth R.K., Nithin Kumar Y.B. and Vasantha M.H.*	**Full Paper**
13:50 – 14:15	**0.5V, Low Power, OTA-C low pass filter for ECG detection** *Rakhi R, Abhijeet D Taralkar, Vasantha M.H and Nithin Kumar Y. B*	**Full Paper**
14:15 – 14:30	**A Novel Opamp and Capacitor Sharing 10 bit 20 MS/s Low Power Pipelined ADC in 0.18um CMOS Technology** *Greeshma R, Anoop V K and Venkataramani B*	**Short Paper**
14:30 – 14:45	**Design of Low Power 4-bit 400MS/s Standard Cell Based Flash ADC** *Mayur S.M, Siddharth R.K., Nithin Kumar Y.B. and Vasantha M.H.*	**Short Paper**
14:45 – 15:00	**A Novel CMOS-based Fully Differential Operational Floating Conveyor** *Hossam Elgemmazy, Amr Helmy, Hassan Mostafa and Yehea Ismail*	**Short Paper**

SPECIAL SESSION 02

Wednesday, July 5th 2017

Emerging Computing Paradigms for Energy-Efficient and Secure IoT Devices

13:00-15:00

Chair:

Himanshu Thapliyal, University of Kentucky, USA

13:00 – 13:25	**Dopingless Transistor based Hybrid Oscillator**	**Full**

	Arbiter Physical Unclonable Function *Venkata P. Yanambaka, Saraju P. Mohanty, Elias Kougianos, Prabha Sundaravadivel, Jawar Singh*	**Paper**
13:25 – 13:50	**Exploiting Memristive Crossbar Memories as Dual-Use Security Primitives in IoT Devices** *Garrett S. Rose, Md. Badruddoja Majumder, and Mesbah Uddin*	**Full Paper**
13:50 – 14:15	**Adiabatic Computing Based Low-Power and DPA-Resistant Lightweight Cryptography for IoT Devices** *Himanshu Thapliyal, T. S. S. Varun and S. Dinesh Kumar*	**Full Paper**

SPECIAL SESSION 03

Wednesday, July 5th 2017

Adaptive Circuits and Systems for Machine Intelligence: The role of adaptive circuits and systems in emerging intelligent systems and networks

13:00-15:00

Chairs:

Theocharis (Theo) Theocharides, Assistant Professor, University of Cyprus

Christos-Savvas Bouganis, Senior Lecturer, Imperial College, London

13:00 – 13:25	**Adaptive and Energy-Efficient Architectures for Machine Learning: Challenges, Opportunities, and Research Roadmap** *Muhammad Shafique, Rehan Hafiz, Lukas Sekanina, Zdenek Vasicek, Vojtech Mrazek*	**Full Paper**
13:25 – 13:50	**Data Stream Processing in Networks-on-Chip** *Jens Rettkowski and Diana Göhringer*	**Full Paper**
13:50 – 14:15	**On how to design dataflow FPGA-based accelerators for Convolutional Neural Networks** *Giuseppe Natale, Marco Basis, M. D. Santambrogio*	**Full Paper**
14:15 – 14:40	**Hardware Acceleration for Machine Learning** *Ruizhe Zhao, Wayne Luk, Xinyu Niu, Huifeng Shi, and Haitao Wang*	**Full Paper**

SESSION 19

Wednesday, July 5th 2017

Analog and Mixed-Signal Circuits III

15:30-17:30

Chair: **Nithin Kumar Yernad Balachandra**

15:30 – 15:55	**A fully integrated fast-response LDO voltage regulator with adaptive transient current distribution** *Xingyuan Tong and Kangkang Wei*	**Full Paper**
15:55 – 15:20	**A 0.32µW, 76.8 dB SNDR Programmable Gain Instrumentation Amplifier for Bio-Potential signal Processing Applications** *Mahesh Kumar Adimulam and Srinivas M.B*	**Full Paper**
15:20 – 15:45	**A Digital Offset Reduction Method for Dynamic Comparators based on Phase Measurement** *Andres Amaya, Javier Ardila and Elkim Roa*	**Full Paper**

SPECIAL SESSION 04

Wednesday, July 5th 2017

Emerging and Secured Applications of IoT

15:30-17:30

Chairs:

Prasun Ghosal, Indian Institute of Engineering Science and Technology, Shibpur, India

Kamalakanta Mahapatra, National Institute of Technology, Rourkela, India

15:30 – 15:55	**Reconfigurable Robust Hybrid Oscillator Arbiter PUF for IoT Security based on DL-FET** *V. P. Yanambaka, S. P. Mohanty, E. Kougianos, P. Sundaravadivel, J. Singh*	**Full Paper**
15:55 – 16:20	**An IoT Enabled Real-Time Communication and Location Tracking System for Vehicular Emergency** *Subha Koley, Prasun Ghosal*	**Full Paper**
13:50 – 14:15	**A Flexible Pay-per Device Licensing Scheme for FPGA IP Cores** *Sudeendra kumar K, Sauvagya Sahoo, Abhishek Mahapatra, Ayas Kanta Swain, K.K.Mahapatra*	**Full Paper**

SPECIAL SESSION 05

Wednesday, July 5th 2017

Innovation in Memory Technologies and Their Applications

15:30-16:45

Chair:

Hai (Helen) Li, Duke University, USA

15:30 – 15:55	**In-Memory Computing with Spintronic Devices** *Deliang Fan, Shaahin Angizi, Zhezhi He, Farhana Parveen*	**Full Paper**
15:55 – 16:20	**Approximate SRAM for Energy-Efficient, Privacy-Preserving Convolutional Neural Networks** *Lita Yang, Boris Murmann*	**Full Paper**
16:20 – 16:45	**Innovative circuits using negative differential resistance property of Tunnel FETs** *Navneet Gupta*	**Full Paper**

POSTER SESSION

Tuesday July 4th, 2017

16:00 - 17:00

1	**CoG: Coarse-grained Grid-based design for near tape-out power estimation accuracy at high level** *Syed Mohammad Asad Hassan Jafri and Ahmed Hemani*
2	**High Speed Power Efficient Carry Select Adder Design** *Raghava Katreepalli and Themistoklis Haniotakis*
3	**A 65 nm, High-Stable Ultra Low-Leakage 11T SRAM Memory Cell Design For IoT Applications** *Vishal Sharma, Pooran Singh, Gopal M and Dr. Santosh Vishvakarma*
4	**Decoupling Translation Lookaside Buffer Coherence from Cache Coherence** *Hao Liu, Quentin Meunier and Alain Greiner*
5	**Centrality Indicators For Efficient And Scalable Logic Masking** *Brice Colombier, Lilian Bossuet and David Hely*
6	**Combined TDM and SDM Circuit Switching NoCs with Dedicated Connection Allocator** *Yong Chen, Emil Matus and Gerhard Fettweis*
7	**Minimizing Critical Access Time for 3D Data Bus Based on Inserted Bus Switches and Repeaters** *Chia-Chun Tsai*
8	**Inverter Propagation and Fan-out Constraints for Beyond-CMOS Majority-based Technologies** *Eleonora Testa, Odysseas Zografos, Mathias Soeken, Adrien Vaysset, Mauricio Manfrini, Rudy Lauwereins and Giovanni De Micheli*
9	**BioViz: An Interactive Visualization Engine for Digital Microfluidic Biochips** *Jannis Stoppe, Oliver Keszocze, Maximilian Luenert, Robert Wille and Rolf Drechsler*
10	**Scouting Logic: A Novel Memristor-Based Logic Design for Emerging Resistive Computing** *Lei Xie, Hoang Anh Du Nguyen, Jintao Yu, Ali Kaichouhi, Mottaqiallah Taouil and Said Hamdioui*
11	**A Meta-Routing Method to Create Multiple Virtual Logical Networks on a Single Hardware NoC** *Hela Belhadj Amor, Hamed Sheibanyrad and Frédéric Petrot*
12	**Secured-by-Design FPGA against Early Evaluation** *Ziyad Almohaimeed and Mihai Sima*
13	**Customizing Skewed Trees for Fast Memory Integrity Verification in Embedded Systems** Saru Vig, Tan Yng Tzer, Guiyuan Jiang and Siew Kei Lam
14	**A Power Efficient System Design Methodology Employing Approximate Arithmetic Units**

	Tuba Ayhan, Fırat Kula and Mustafa Altun
15	**Detection of Layout-Level Trojans by Monitoring Substrate with Preexisting Built-in Sensors** *Leonel Acunha Guimarães, Rodrigo Possamai Bastos and Laurent Fesquet*
16	**Coding for Efficient Caching in Multicore Embedded Systems** *Tosiron Adegbija and Ravi Tandon*
17	**A Workload Characterization for the Internet of Medical Things (IoMT)** *Ankur Limaye and Tosiron Adegbija*
18	**Offset Analysis and Design Optimization of a Dynamic Sense Amplifier for Resistive Memories** *Salmen Mraihi, Elmehdi Boujamaa, Cyrille Dray and Jacques-Olivier Klein*
19	**Efficient Metastability-Containing Multiplexers** *Stephan Friedrichs and Attila Kinali*
20	**Micro Latch-up Analysis on Ultra-Nanometer VLSI Technologies: A new Monte Carlo Approach** *Luca Sterpone and Sarah Azimi*
21	**Serial ATA Commands Logger for Security Monitoring on FPGA Devices** *Dan Cristian Turicu, Octavian Cret and Lucia Vacariu*
22	**PACT: Priority-Aware Phase-based Cache Tuning for Embedded Systems** *Sam Gianelli and Tosiron Adegbija*
23	**CAPSL: The Component Authentication Process for Sandboxed Layouts** *Taylor Whitaker and Christophe Bobda*
24	**Layout Vulnerability Reduction against Trojan Insertion using Security-aware White Space Distribution** *Hamed Hossein-Talaee and Ali Jahanian*
25	**On Tolerating Faults of TSV/Microbumps for Power Delivery Networks in 3D IC** *Sheng-Hsin Fang, Chang-Tzu Lin, Wei-Hsun Liao, Chien-Chia Huang, Li-Chin Chen, Hung-Ming Chen, I-Hsuan Lee, Ding-Ming Kwai and Yung-Fa Chou*
26	**WT-CTS: Incremental Delay Balancing Using Parallel Wiring Type For CTS** *Scott Lerner and Baris Taskin*
27	**Automatic Assertion Generation for Simulation, Formal Verification and Emulation** *Tong Zhang, Daniel Saab and Jacob A. Abraham*
28	**A 0.3V Low Cost Low Power 24 GHz Low Noise Amplifier with Body Bias Technology** *Ming-Yu Huang, Ren-Yuan Huang and Ro-Min Weng*
29	**Capacitor Mismatch Calibration Technique to Improve the SFDR of 14-bit SAR ADC** *Hua Fan, Franco Maloberti, Dagang Li, Daqian Hu, Yuanjun Cen and Hadi Heidari*
30	**Design of an Asynchronous Detector with Priority Encoding Technique** *Keunyeol Park, Ohoon Kwon, Hyunseob Noh, Minhyun Jin and Minkyu Song*
31	**WT-CTS: Incremental Delay Balancing Using Parallel Wiring Type For CTS**

	Scott Lerner and Baris Taskin
32	**Semiformal Verification of Software-controlled Connections** *Tomas Grimm, Djones Lettnin and Michael Huebner*
33	**A Novel Opamp and Capacitor Sharing 10 bit 20 MS/s Low Power Pipelined ADC in 0.18um CMOS Technology** *Greeshma R, Anoop V K and Venkataramani B*
34	**Design of Low Power 4-bit 400MS/s Standard Cell Based Flash ADC** *Mayur S.M, Siddharth R.K., Nithin Kumar Y.B. and Vasantha M.H.*
35	**A Novel CMOS-based Fully Differential Operational Floating Conveyor** *Hossam Elgemmazy, Amr Helmy, Hassan Mostafa and Yehea Ismail*