IEEE Computer Society Annual Symposium on VLSI

ISVLSI 2018

8-11 July 2018 Hong Kong

Welcome to ISVLSI 2018

Program Overview

General Information

Registration Hours & Location

- Sunday, July 8, Staff Club, 6pm -8pm
- Monday, July 9, N103, 7:30am – 6pm
- Tuesday, July 10, N103, 7:30am – 6pm
- Wednesday, July 11, N103, 8am – 6pm

Proceedings

ISVLSI Conference papers will be delivered electronically online through the following link. We have sent you the login ID and password through your registered email address.

http://conferences.computer.org/isvlsi/2018

WIFI Network

The user with eduroam account will connect automatically. There is also WiFi network "Wi-Fi.HK via PolyU" for free access.

Speaker Breakfast

The speaker breakfast will be held in the room of *N103* at the following time slots. Bread, sandwich and cold drink including water and juice will be provided.

- Monday, July 9, 7:30am – 8:10am
- Tuesday, July 10, 7:30am – 8:15am
- Wednesday, July 11, 7:45am – 8:30am

Assembly Point for Lunch, Banquet and Cruise

We will first assemble at the following place and the student helper will lead us to the restaurant for lunches or to the bus stop for coach boarding. If you prefer, you can also go to the lunch restaurant or coach bus stop by yourself. We have included the map for your reference.

Assemble place: In front of *N003*

Assemble time:

- 11:50am for the lunch
- 7:10pm for the Cruise on July 9th
- 6:20pm for the Banquet on July 10th

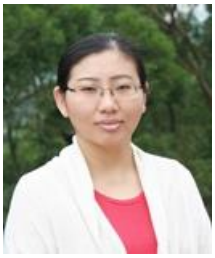
Message from the General Chairs

ISVLSI 2018

It is our great pleasure to welcome all the participants to the 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI, http://www.isvlsi.org/) held at Hong Kong, China. The main goal of ISVLSI is to explore emerging trends and novel ideas and concepts in the area of VLSI and provide a platform for both academic and industrial researchers to interact under one roof for research and development which may lead to realization of efficient, robust, and secure VLSI circuits and systems. ISVLSI has been initiated as a sponsored meeting of Technical Committee on VLSI (TCVLSI, http://www.ieee-tcvlsi.org/), of IEEE Computer Society (IEEE-CS) and we are sure that from the active co-operation of all volunteers ISVLSI got an excellent start. It may be noted that TCVLSI is one among 26 technical committees/councils of IEEE-CS which endorse different meetings in the scope of IEEE-CS. TCVLSI endorses a league of successful meetings such as ARITH, ASAP, iNIS, IWLS, and SLIP. ISVLSI 2018 is sponsored by IEEE-CS through TCVLSI and technically co-sponsored by IEEE-CAS as well as IEEE-CEDA. ISVLSI 2018 proceedings is published by IEEE-CS conference publication services (CPS). ISVLSI has attracted attendees from all over the globe. We hope that ISVLSI will continue attracting renowned people from various parts of the globe and continue serving the community in its future years.

ISVLSI 2018 will be hosted at the Hong Kong Polytechnic University. Hong Kong, located at the mouth of the Pearl River Delta in Southern China and bordered by the Shenzhen Special Economic Zone to the north, is a major financial and services center featuring state-of-the-art infrastructure and highly efficient business services. Its stock market is Asia's third-largest one in terms of market capitalization, only behind the Tokyo Stock Exchange and Shanghai Stock Exchange, and the sixth largest in the world. Frequently described as a place where "East meets West", Hong Kong is a cosmopolitan metropolis where traditional Chinese culture blends perfectly with Western culture. Hong Kong is also one global hub for higher education, with one of the world's most impressive concentrations of internationally renowned institutions. We hope that you will spend several days and enjoy the historical and modern monuments of the city and its surrounding regions.

The general chairs would like to thank the steering committee for supporting ISVLSI 2018. We would like to thank the Hong Kong Polytechnic University and other sponsors in helping ISVLSI 2018. ISVLSI 2018 will have 6 keynotes, 5 plenary talks and 32 sessions from high quality researchers around the globe. We would like to specifically thank the keynote and speakers for their support and exciting talks to the ISVLSI 2018 attendee. We would like to specifically thank the program chairs, Hai (Helen) Li, Yu Wang, and Wujie Wen for their excellent job in selecting quality papers for presentations. We would sincerely thank the special session chairs, publication chair, finance chairs, web chair, publicity chairs, local arrangement chair, student symposium chair, registration chairs, and all other active volunteers, for their fantastic job in running the symposium. We would like to thank the sponsors for supporting ISVLSI 2018.



General Co-Chair, **Wei Zhang**
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Hong Kong
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General Co-Chair, **Chun Jason Xue**
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General Co-Chair, **Zili Shao**
Hong Kong Polytechnic University, Hong Kong
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Message from the Technical Program Chairs

ISVLSI 2018

It is with great pleasure that we welcome you to the 17th IEEE Computer-Society Symposium on VLSI (ISVLSI 2018, http://www.eng.ucy.ac.cy/theocharides/isvlsi18/) in the city, Hong Kong SAR, China. ISVLSI is a sister conference of a league of successful meetings such as ARITH, ASAP, iNIS, IWLS, and SLIP which are sponsored by the Technical Committee on VLSI (TCVLSI, http://www.ieee-tcvlsi.org/), of IEEE Computer Society (IEEE-CS). ISVLSI explores emerging trends and novel ideas and concepts in the area of VLSI. Over more than a decade the ISVLSI has been a unique forum promoting multidisciplinary research and new visionary approaches in the area of VLSI. The ISVLSI brings together leading scientists and researchers from academia and industry. The papers from this symposium have been published as the special issue to top archival journals and for the ISVLSI 2018 selected papers will be invited for consideration in special issues in the IEEE Transactions on Nanotechnology (TNANO) and IEEE Consumer Electronics Magazine. This is one of the facts that indicate a very high quality of the ISVLSI papers, and we are determined to keep a strong emphasis on this critical aspect of any conference. The symposium proceedings are published by IEEE-CS conference publication services (CPS).

ISVLSI 2018 covers a range of topics: from VLSI circuits, systems and design methods to system level design and system-on-chip (SoC) issues, to bringing VLSI experience to new areas, architectures, and technologies. Future design methodologies as well as new Electronic Design Automation (EDA) tools to support them will also be the key topics. ISVLSI 2018 papers are in the following 6 tracks:

1) Analog and Mixed-Signal Circuits (AMS)
2) Computer-Aided Design and Verification (CAD)
3) Digital Circuits and FPGA based Designs (DCF)
4) Emerging and Post-CMOS Technologies (EPT)
5) System Design and Security (SDS)
6) Testing, Reliability, and Fault-Tolerance (TRF)

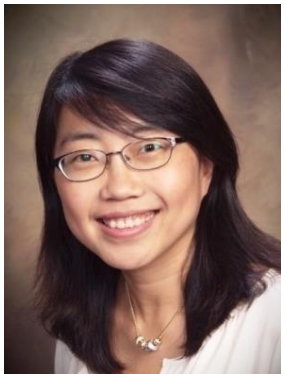
ISVLSI 2018 papers can be divided into two separate categories: regular papers and special session papers. The regular session papers have been selected after a rigorous review process. The special session papers have been by invitation from the established researchers from different areas of VLSI, which have also been reviewed by special session chairs and individual special session proposers. Due to the time constraints the papers are either selected oral presentation or poster presentations. However, both oral and poster presentation papers got 6-page budget in the proceedings. This is one of the unique aspects that the accepted papers get similar importance in the proceedings. In addition, ISVLSI 2018 also has a Student Research Forum (SRF) in which the papers are presented as posters and appear in proceedings as 6-page papers. The SRF papers have gone through a different review process by the SRF chairs and other volunteers.

The ISVLSI 2018 has received a very good response for the manuscript submission. The submissions were received from all parts of the globe, with major submissions from United States of America (USA), India, China, Singapore, Japan, Taiwan and Switzerland. Due to time constraints in the 3-day event, ISVLSI 2018 could only accept limited number of papers of high quality. ISVLSI 2018 received 192 submissions, out of these **54** high quality papers are accepted for oral presentation and the proceedings. These are divided into **18** oral sessions. Thus making an acceptance ratio of 29%. This shows the quality and competitiveness of the conference. All submitted papers had undergone double-blind-review process by a strong team of leading experts from around the globe in respective fields and the program committee members and additional reviewers. There are **50** special session oral presentations from prominent authors divided into **14** sessions. In addition, a poster session contains **35** posters from general pool and **6** posters Student Research Forum will enrich the technical discussions.

The success of this magnitude is not possible without since help from various volunteers. We wish to express our sincere appreciation to the hardworking track chairs, dedicated members of the Technical Program Committee and additional reviewers. We also thank the authors and invited speakers for their contributions to an outstanding technical program. Our special thanks go to the Steering Committee and Organizing Committee members of ISVLSI 2018 for their support and cooperation. We acknowledge the high quality editing work of production editor of the IEEE Computer Society Conference Publishing Services for the high-quality and timely production of the ISVLSI 2018 Proceedings.

We wish you a very productive ISVLSI 2018 and hope you will find papers presented at the ISVLSI 2018 to be a valuable source of reference for your current and future research. We hope your stay during the ISVLSI 2018 at Hong Kong, will be an enjoyable experience and help in professional networking.

We also look forward to your participation in ISVLSI 2019 next year to be held at Miami, Florida, USA.



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Program Chair
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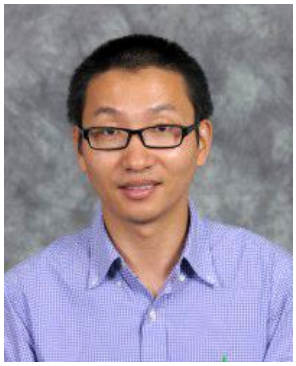


Program Chair
Wujie Wen. Florida International University, USA. wwen@fiu.edu

Technical Program Committee

ISVLSI 2018

Digital Circuits and FPGA based Design Track

Dimitrios Soudris	*National Technical University of Athens*
Xinying Wang	*Intel Programmable Solution Group*
Yu Bai	*California State University Fullerton*
Rakesh Kumar	*zGlue Inc*
Hailong Jiao	*Peking University*
Christophe Bobda	*University of Arkansas*
Liang Men	*University of Arkansas*
Li Zhang	*Technical University of Munich*
Deliang Fan	*University of Central Florida*
Jinhui Wang	*North Dakota State University*
Na Gong	*North Dakota State University*
Zheng Wang	*Shenzhen Institutes of Advanced Technology*
Ronald Demara	*University of Central Florida*
Yingjie Lao	*Clemson University*
Eric Liang	*Peking University*
Miaoqing Huang	*University of Arkansas*
Chien-Wei Lo	*University of Arkansas*
David Bol	*Université catholique de Louvain*
Ann Gordon-Ross	*University of Florida*
Chun-Yi Lee	*National Tsinghua University*
Weiqiang Liu	*Nanjing University of Aeronautics and Astronautics*
Hao Zheng	*University of South Florida*
Balatsoukas-Stimming Alexios	*Ecole Polytechnique Fédérale de Lausanne*
Christophe Jego	*IMS Laboratory*

Computer-Aided Design and Verification Track

Kunal Ganeshpure	*Mentor Graphics Corporation*
Vivek Chaturvedi	*Nanyang Technological University*
Weize Yu	*Old Dominion University*
Xiaowei Xu	*University of Notre Dame*
Shouyi Yin	*Tsinghua University*
Theocharis Theocharides	*University of Cyprus*
Nagi Naganathan	*Avago Technologies*
Miroslav Velev	*Aries Design Automation*

Emerging and Post-CMOS Technologies Track

Mahdi Nikdast	*Colorado State University*
Prasun Ghosal	*Indian Institute of Engineering Science and Technology, Shibpur*
Himanshu Thapliyal	*University of Kentucky*
Sharad Sinha	*Nanyang Technological University*
Yuanqing Cheng	*Beihang University*
Xiaoming Chen	*Institute of Computing Technology, Chinese Academy of Sciences*
Garrett Rose	*University of Tennessee*
Lionel Torres	*LIRMM*
Chenchen Liu	*Clarkson University*
Nezih Pala	*Florida International University*
Jiang Xu	*Hong Kong University of Science and Technology*
Thomas Mikolajick	*NaMLab / TU Dresden*
Saraju Mohanty	*University of North Texas*

System Design and Security Track

Upasna Vishnoi	*Marvell Semiconductor Inc.*
Luciano Ost	*Loughborough University*
Naghmeh Karimi	*University of Maryland, Baltimore County (UMBC)*
Chen Liu	*Intel*
Madhu Mutyam	*Indian Institute of Technology, Madras*
Keni Qiu	*Capital Normal University*
Arslan Munir	*Kansas State University*
Rance Rodrigues	*University of Massachusetts at Amherst*
Arun Kanuparthi	*Intel*
Fabio Campi	*Silicon Biosystems*
Tanguy Risset	*Citi, INSA-Lyon*
Michail Maniatakos	*New York University*
Marco Wehrmeister	*Federal University of Technology - Parana*
Fernando Moraes	*Pontifical Catholic University of Rio Grande do Sul*
Edoardo Fusella	*UNINA*
Apostolos Fournaris	*Technological Educational Institute of Western Greece*
Ricardo Chaves	*IST / INESC-ID*
Sicheng Li	*Hewlett-Packard (HP)*
Yarui Peng	*University of Arkansas*
Ramesh Karri	*polytechnic institute of NYU*
Mateus Rutzig	*Federal University of Santa Maria*
Nicolas Sklavos	*University of Patras*
Sheng Wei	*University of Nebraska–Lincoln*
Guy Gogniat	*Université de Bretagne Sud - UEB*
Nele Mentens	*Katholieke Universiteit Leuven*
David Hely	*Grenoble INP*
Fei Wu	*Huazhong University of Science and Technology*
Yier Jin	*University of Florida*

Testing, Reliability and Fault-Tolerance Track

Mihalis Psarakis	*University of Piraeus*
Matteo Sonza Reorda	*Politecnico di Torino*
Ernesto Sanchez	*Politecnico di Torino*
Xiaoqing Wen	*Kyushu Institute of Technology*
Alessandro Savino	*Politecnico di Torino*
Giorgio Di Natale	*LIRMM*
Eduardo Bezerra	*UFSC*
Elena Ioana Vatajelu	*INP - TIMA Laboratory*
Luigi Dilillo	*LIRMM*
Stefano Di Carlo	*Politecnico di Torino*
Leticia Bolzani Poehls	*Catholic University of Rio Grande do Sul (PUCRS)*
Zebo Peng	*Linkoping University*
Yongfu Li	*GLOBALFOUNDRIES, Singapore*
Michele Portolan	*TIMA*
Dong Xiang	*Tsinghua University*

Analog and Mixed-Signal Circuits Track

Bo Jiang	*OmniVision Technologies, Inc*
Jose Pineda De Gyvez	*NXP Semiconductors*
Munem Hossain	*University of Missouri – Kansas City*
Elias Kougianos	*University of North Texas*
Chi Zhang	*GlobalFoundries*
Aisha Alhammadi	*University of Sharjah*
Manish Goswami	*Indian Institute of Information Technology*
Chuang Zhang	*Broadcom*
Maryam Shojaei Baghini	*India Institute of Technology, Bombay*
Steffen Paul	*University Bremen*

Student Research Forum Track

Anupam Chattopadhyay	*Nanyang Technological University Singapore*
Zheng Wang	*Shenzhen Institutes of Advanced Technology*

Keynote 1

8:30am ~ 9:30am, Monday July 9, 2018

Future Hybrid Circuits for Functionality, Performance and Energy Efficiency

K.-T. Tim Cheng
Professor, Dean of School of Engineering
Department of Electronic and Computer Engineering
Hong Kong University of Science and Technology

Summary
Advances in photonics, flexible electronics, emerging memories, etc. and Si electronics' integration with these devices have enabled new classes of integrated circuits and systems with enhanced functionality, higher performance, or lower power consumption. Driving greater integration of such heterogeneous hybrid chips/systems can facilitate the continued proliferation of low-cost micro-/nano-systems for a wide range of applications. However, achieving their large-scale integration will require design ecosystem and design automation tools/methodologies much like those that enabled electronic integration in previous decades.

In this talk, I will briefly introduce two recent Manufacturing Innovation Institutes, on Integrated Photonics and on Flexible Hybrid Electronics respectively, and a research center on developing 3D Hybrid CMOS-memristor circuits, which bring together academia, industry, and government partners to increase design and manufacturing competitiveness in these areas. I will then describe some of our recent results and highlight the needs, challenges and opportunities in these areas.

About K.-T. Tim Cheng
K.-T. Tim Cheng received his Ph.D. in EECS from the University of California, Berkeley in 1988. He has been serving as Dean of Engineering and Chair Professor of ECE and CSE at Hong Kong University of Science and Technology (HKUST) since May 2016. He worked at Bell Laboratories from 1988 to 1993 and joined the faculty at Univ. of California, Santa Barbara in 1993 where he was the founding director of UCSB's Computer Engineering Program (1999-2002), Chair of the ECE Department (2005-2008) and Associate Vice Chancellor for Research (2013-2016). His current research interests include design automation for photonics IC and flexible hybrid circuits, memristive memories, mobile embedded systems, and mobile computer vision. He has co-authored five books, supervised 50 PhD theses, held 12 U.S. Patents, and published extensively in these areas. He served as Director for US Department of Defense MURI Center for 3D hybrid circuits which aims at integrating CMOS with high-density memristors.

Cheng, an IEEE fellow, received 10+ Best Paper Awards from various IEEE and ACM conferences and journals. He has also received UCSB College of Engineering Outstanding Teaching Faculty Award. He served as Editor-in-Chief of IEEE Design and Test of Computers and was a board member of IEEE Council of Electronic Design Automation's Board of Governors and IEEE Computer Society's Publication Board.

Keynote 2

1:30pm ~ 2:30pm, Monday July 9, 2018

Low Power High Performance Multicore Hardware and Software Co-Design

Hironori Kasahara
President of IEEE Computer Society
Professor, Department of Computer Science and Engineering
Waseda University

Summary
Multicores have been attracting much attention to improve performance and reduce power consumption of computing systems, from embedded to supercomputing systems. To obtain high performance and low power on multicores, co-design of hardware and software is essential. Especially architecture supports for parallelizing and power reducing compiler are very important. This talk first introduces a parallelizing, memory usage optimizing and power reducing compiler and its performance on various multicores from Intel, IBM, arm, Fujitsu, Infineon, and Renesas for various applications including multimedia, automobile, cancer treatment, and earthquake simulation. It next explains architecture supports for the compiler, such as, global address space, data and group barrier synchronization, vector accelerators, data transfer controllers, and power control using DVFS and Clock and Power Gating. The hardware and software co-design allows us not only high performance and low power but also short development period and low development cost of parallel software.

About Hironori Kasahara
Hironori Kasahara is an IEEE Computer Society President 2018 and a professor in the Department of Computer Science and Engineering at Waseda University. He is an IEEE Fellow, an IPSJ Fellow, a Golden Core Member of the IEEE Computer Society, a professional member of the IEEE Eta Kappa Nu, a member of the Engineering Academy of Japan and the Science Council of Japan. He received a PhD in 1985 from Waseda University, Tokyo, joined its faculty in 1986, and has been a professor of computer science since 1997 and a director of the Advanced Multicore Research Institute since 2004. He was a visiting scholar at University of California, Berkeley, and the University of Illinois at Urbana–Champaign's Center for Supercomputing R&D.

He has served as a chair or member of 250 society and government committees, including a member of the CS Board of Governors and Executive Committee; chair of CS Planning Committee, Constitution & Bylaws Committee, Multicore STC and CS Japan chapter; associate editor of IEEE Transactions on Computers; vice PC chair of the 1996 ENIAC 50th Anniversary International Conference on Supercomputing; general chair of LCPC; PC member of SC, PACT, and ASPLOS; board member of IEEE Tokyo section; and member of the Earth Simulator and K supercomputer committees. Kasahara received the CS Golden Core Member Award, IFAC World Congress Young Author Prize, Sakai Special Research Award, and the Japanese Minister's Science and Technology Prize. He led Japanese national projects on parallelizing compilers and embedded multicores, and has presented 215 papers, 155 invited talks, and 30 patents. His research has appeared in 557 newspaper and Web articles.

Keynote 3

8:30am ~ 9:30am, Tuesday July 10, 2018

Machine Learning Further Improve Physical Design PPA at Advanced Node

Weibin Ding
Cadence Software Engineering Group Director
Head of Cadence Global AI Center of Digital and Signoff Group

Summary
Place and route at advanced process node is becoming much more complicated than ever, to meet both timing and DRC closure need multiple core engines to co-work seamlessly well. Traditionally it is very hard problem to decide a solution finally works or not along the flow, the machine learning method opens a door to give better correlated result in the flow. We have constantly seen the improvement trend in our product development.

About Weibin Ding
Weibin is based in Shanghai – the APAC Headquarter of Cadence and currently leading the Global AI Center of DSG which is a new strategic function in Cadence since January 2018. Prior to that, he led 100+ software engineers responsible for Innovus product development. He initiated the Machine Learning direction for Innovus in early 2015 and responsible for making it production. He has been working at Cadence for 12 years and held 3 US patents.

Weibin received a B.S. and M.S. degree in Computer Science from Shanghai Jiao Tong University.

Keynote 4

1:30pm ~ 2:30pm, Tuesday July 10, 2018

Power Density and Circuit Aging – System-Level Means for Mitigation

Jörg Henkel
Chair of Embedded System
Professor of Computer Science
Karlsruhe Institute of Technology (KIT), Germany

Summary
Power density will stay a major challenge for the foreseeable future. Despite orders-of-magnitude-improved efficiency, power consumption per area is rising, mainly due to the limits of voltage scaling. To investigate the physical implications of high power densities, we must distinguish between peak and average temperatures and temporal and spatial thermal gradients because they trigger circuit-aging mechanisms and eventually jeopardize the reliability of an on-chip system.

The talk starts by presenting some basic interdependencies in the triangle of power density, circuit aging and reliability and continues with solutions to mitigate the problem via, among others, power density-aware resource management, thermal save power (TSP), efficient power budgeting as well as "Aging Aware Boosting.

About Jörg Henkel
Jörg Henkel (M'95-SM'01-F'15) received the master's and PhD (Summa cum laude) degrees from the Technical University of Braunschweig, Germany. He is with the Karlsruhe Institute of Technology (KIT), Germany. Before he worked at the NEC Laboratories, Princeton, NJ. His current research interests include design and architectures for embedded systems with focus on low power and reliability. He has received various research awards, among them the 2008 DATE Best Paper Award, the 2009 IEEE/ACM William J. Mc Calla ICCAD Best Paper Award, the CODES+ISSS 2011, 2014 and 2015 Best Paper Awards. He was the general chair of major CAD events incl. ICCAD and ESWeek. He is the chairman of the IEEE Computer Society, Germany Section, and was the editor-in-chief of the ACM Transactions on Embedded Computing Systems for two terms. He is currently the editor-in-chief of the IEEE Design and Test Magazine. He is also an Initiator and Spokesperson of the national priority program on Dependable Embedded Systems of the German Science Foundation and the site coordinator (Karlsruhe site) of the three-university collaborative research center on invasive computing. He is a Fellow of the IEEE and holds ten US patents.

Keynote 5

8:30am ~ 9:30am, Wednesday July 11, 2018

Self-Awareness for Heterogeneous MPSoCs: A Case Study using Adaptive, Reflective Middleware

Nikil Dutt
Center for Embedded and CyberPhysical Systems (CECS)
Center for Cognitive Neuroscience and Engineering (CENCE)
Chancellor's Professor, Department of Computer Science, University of California, Irvine

Summary
Self-awareness has a long history in biology, psychology, medicine, engineering and (more recently) computing. In the past decade this has inspired new self-aware strategies for emerging computing substrates (e.g., complex heterogeneous MPSoCs) that must cope with the (often conflicting) challenges of resiliency, energy, heat, cost, performance, security, etc. in the face of highly dynamic operational behaviors and environmental conditions. Earlier we had championed the concept of ***CyberPhysical-Systems-on-Chip (CPSoC)***, a new class of sensor-actuator rich many-core computing platforms that intrinsically couples on-chip and cross-layer sensing and actuation to enable self-awareness. Unlike traditional MPSoCs, CPSoC is distinguished by an intelligent co-design of the control, communication, and computing (C3) system that interacts with the physical environment in real-time in order to modify the system's behavior so as to adaptively achieve desired objectives and Quality-of-Service (QoS). The CPSoC design paradigm enables self-awareness (i.e., the ability of the system to observe its own internal and external behaviors such that it is capable of making judicious decision) and (opportunistic) adaptation using the concept of cross-layer physical and virtual sensing and actuations applied across different layers of the hardware/software system stack. The closed loop control used for adaptation to dynamic variation -- commonly known as the observe-decide-act (ODA) loop -- is implemented using an adaptive, reflective middleware layer.
In this talk I will present a case study of this adaptive, reflective middleware layer using a holistic approach for performing resource allocation decisions and power management by leveraging concepts from reflective software. Reflection enables dynamic adaptation based on both external feedback and introspection (i.e., self-assessment). In our context, this translates into performing resource management actuation considering both sensing information (e.g., readings from performance counters, power sensors, etc.) to assess the current system state, as well as models to predict the behavior of other system components before performing an action. I will summarize results leveraging our adaptive-reflective middleware toolchain to i) perform energy-efficient task mapping on heterogeneous architectures, ii) explore the design space of novel HMP architectures, and iii) extend the lifetime of mobile devices.

About Nikil Dutt
Nikil Dutt is a Chancellor's Professor of CS, Cognitive Sciences, and EECS at the University of California, Irvine. He received a PhD from the University of Illinois at Urbana-Champaign (1989). His research interests are in embedded systems, EDA, computer architecture and compilers, distributed systems, and brain-inspired architectures and computing. He has received numerous best paper awards and is coauthor of 7 books. Professor Dutt has served as EiC of ACM TODAES and AE for ACM TECS and IEEE TVLSI. He is on the steering, organizing, and program committees of several premier EDA and Embedded System Design conferences and workshops, and has also been on the advisory boards of ACM SIGBED, ACM SIGDA, ACM TECS and IEEE ESL. He is an ACM Fellow, IEEE Fellow, and recipient of the IFIP Silver Core Award.

Keynote 6

1:30pm ~ 2:30pm, Wednesday July 11, 2018

Cogntive Vision Systems: Energy Efficiency Influences from Algorithms to Architectures

Vijaykrishnan Narayanan
Distinguished Professor, Computer Science and Engineering and Electrical Engineering
The Pennsylvania State University

Summary
Shopping is widely considered as a relaxing leisure activity. However, grocery shopping can be a frustrating experience for those with visual impairment. While getting to a grocery shop itself is not as much of a challenge for them, locating and picking the items in the grocery shelf becomes a task as challenging as picking a needle from the haystack. Imagine picking up five items for your dinner recipe from a typical grocery store in the US that carries around 35,000 unique items and can have more than 30 aisles spanning 45,000 square meters. This talk will showcase synergistic advances in algorithms, architectures and interface design for assisting those with visual impairment to do shopping. The talk will focus on multiple energy-efficient solutions that consider the battery life time of the vision system.

About Vijaykrishnan Narayanan
Vijay Narayanan is a Distinguished Professor of Computer Science and Engineering and Electrical Engineering at The Pennsylvania State University. He is the director of the NSF Expeditions-in-Computing Program on Visual Cortex on Silicon and a thrust leader for the JUMP Center on Brain-Inspired Computing. He has published more than 400 papers and won several awards in recognition of his research in power-aware systems, embedded systems and computer architecture. He is a fellow of IEEE and ACM.

Plenary Talk 1

2:30pm ~ 3:00pm, Monday July 9, 2018

Achieving 19 TFLOPS in 10W for deep learning using network pruning on Xilinx Zynq Ultrascale+ FPGA

Yi Shan
CTO and Partner of DeePhi Tech

Summary
Deep learning algorithms such as Convolution Neural Network (CNN) is fast becoming the critical part of image perceptions in embedded vision applications in the automotive, drones, surveillance and industrial vision markets. Applications include multi-object detection, semantic segmentation and image classification. However, when scaling these networks to modern resolutions like HD and 4K, the computational requirements for real-time system could easily go over 10 TFLOPS consuming hundreds of watts of power, which is simply unacceptable for most edge applications. In this talk, we will describe a network/weight pruning methodology that achieves over 10 times performance gain on Zynq Ultrascale+ with very small accuracy loss. The network inference running on Zynq Ultrascale+ has achieved 19 TFLOPS-equivalent of the original SSD network in less than 10W.

About Yi Shan
Yi Shan graduated from Tsinghua University with a Ph.D. degree in Electronic Science and Technology. He was joint educated at Imperial College London. He has been engaged in research work at Microsoft Research, IBM Research and Baidu Research. He was selected as an outstanding talents program in Beijing.
Dr. Shan is the CTO and partner of DeePhi Tech and fully responsible for the technical development and the management of engineering and production teams. In the development and application of the original innovation technology in frontier industries such as artificial intelligence, he has achieved a number of scientific and technological achievements. He led the team to develop DPUs (Deep Processing Units) and its hardware and software systems for AI applications. Based on this, they formed two key directions for deep learning accelerated on FPGA modules and ASIC. Now DeePhi's products are widely used in smart surveillance, data center, ADAS (advanced driver assistance systems) and other fields.

Plenary Talk 2

3:00pm ~ 3:30pm, Monday July 9, 2018

Overcoming Challenges of Accelerating Deep Neural Network Computations

Deming Chen
Donald Biggar Willett Scholar
Professor, Electrical and Computer Engineering
University of Illinois Urbana-Champaign

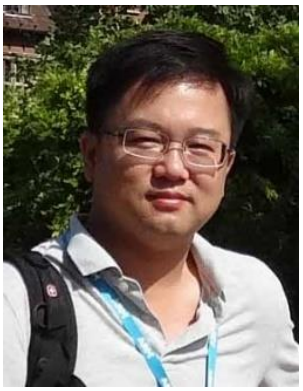
Summary
Deep Neural Networks (DNNs) are computation intensive. Without efficient hardware implementations of DNNs, many promising AI applications will not be practically realizable. In this talk, we will analyze several challenges facing the AI community for mapping DNNs to hardware accelerators. Especially, we will evaluate FPGA's potential role for accelerating DNNs for both the cloud and edge devices. Although FPGAs can provide desirable customized hardware solutions, they are difficult to program and optimize. We will present a series of effective design techniques for implementing DNNs on FPGAs with high performance and energy efficiency. These include automated hardware/software co-design, the use of configurable DNN IPs, resource allocation across DNN layers, smart pipeline scheduling, Winograd and FFT techniques, and DNN reduction and re-training. We showcase several design solutions including Long-term Recurrent Convolution Network (LRCN) for video captioning, Inception module (GoogleNet) for face recognition, as well as Long Short-Term Memory (LSTM) for sound recognition. We will also present some of our recent work on developing new DNN models and data structures for achieving higher accuracy for several interesting applications such as crowd counting, genomics, and music synthesis.

About Deming Chen
Dr. Deming Chen obtained his BS in computer science from University of Pittsburgh, Pennsylvania in 1995, and his MS and PhD in computer science from University of California at Los Angeles in 2001 and 2005 respectively. He joined the ECE department of University of Illinois at Urbana-Champaign (UIUC) in 2005 and has been a full professor in the same department since 2015. His current research interests include system-level and high-level synthesis, machine learning, computational genomics, GPU and reconfigurable computing, and hardware security. He has given about 100 invited talks sharing these research results worldwide. Dr. Chen is a technical committee member for a series of top conferences and symposia on EDA, FPGA, low-power design, and VLSI systems design. He is an associated editor for several leading IEEE and ACM journals. He received the NSF CAREER Award in 2008, the ACM SIGDA Outstanding New Faculty Award in 2010, and IBM Faculty Award in 2014 and 2015. He also received seven Best Paper Awards and the First Place Winner Award of DAC International Hardware Contest on IoT in 2017. He is included in the List of Teachers Ranked as Excellent in 2008 and 2017. He was involved in two startup companies previously, which were both acquired. In 2016, he co-founded a new startup, Inspirit IoT, Inc., for design and synthesis for machine learning applications targeting the IoT industry. He is the Donald Biggar Willett Faculty Scholar of College of Engineering of UIUC.

Plenary Talk 3

2:30pm ~ 3:00pm, Tuesday July 10, 2018

The Advanced Technologies in the New Generation of Phytium's Processors -- From the Architecture to Implementation



Zhuo Ma
Deputy General Manager
SoC R&D Center of Phytium

Summary
In the past decades, the computer technology comes to a rapid increasing new ear, and the silicon-based high performance processors give the main impetus. To be a member of the first group of CPU design houses, Phytium Technology Co., Ltd. is a fast-growing Chinese IC design company, and is dedicated to design, manufacture high performance and low power CPU chips as well as services around the products.

About Zhuo Ma
Dr. Ma is the deputy general manager of SoC R&D center of Phytium. In the past two decades, Dr. MA focused on the technologies of the implementation of high performance processors. He is leading a group of gifted engineers to build the most high performanced ARM-based CPU chips. In the presentation, He will introduce the advanced design technologies of Phytium's CPUs, and share a lot of successful stories.

Plenary Talk 4

3:00pm ~ 3:30pm, Tuesday July 10, 2018

Security of the Internet of Things: Can Hardware Change the Game?

Swarup Bhunia
Professor, Electrical and Computer Engineering
University of Florida, Gainesville, Florida

Summary
Security has become a critical design challenge for modern electronic hardware. With the emergence of the Internet of Things (IoT) regime that promises exciting new applications from smart cities to connected autonomous vehicles, security has come to the forefront of the system design process. Recent discoveries and reports on numerous security attacks on microchips and circuits violate the well-regarded concept of hardware trust anchors. It has prompted system designers to develop wide array of design-for-security and test/validation solutions to achieve high security assurance for electronic hardware, which supports the software stack. At the same time, emerging security issues and countermeasures have also led to interesting interplay between security, verification, and interoperability. Verification of hardware for security and trust at different levels of abstraction is rapidly becoming an integral part of the system design flow. The global economic trend that promotes outsourcing of design and fabrication process to untrusted facilities coupled with the prevalent practice of system on chip design using untrusted 3rd party intellectual property blocks (IPs), has given rise to the critical need of trust verification of IPs, system-on-chip design, and fabricated chips. The talk will also cover spectrum of security challenges for IoTs and describe emerging solutions in creating secure trustworthy hardware that can enable IoT security for the mass.

About Swarup Bhunia
Swarup Bhunia is a preeminence professor of cybersecurity and Steven Yatauro endowed faculty fellow of Computer Engineering at University of Florida, FL, USA. Earlier he was appointed as the T. and A. Schroeder associate professor of Electrical Engineering and Computer Science at Case Western Reserve University, Cleveland, OH, USA. He has over twenty years of research and development experience with 250+ publications in peer-reviewed journals and premier conferences and six authored/edited books. His research interests include hardware security and trust, adaptive nanocomputing and novel test methodologies. Dr. Bhunia received IBM Faculty Award (2013), National Science Foundation career development award (2011), Semiconductor Research Corporation Inventor Recognition Award (2009), and SRC technical excellence award (2005) as a team member, and several best paper awards/nominations. He is co-founding editor-in-chief of a Springer journal on hardware and systems security. He has been serving as an associate editor of IEEE Transactions on CAD, IEEE Transactions on Multi-Scale Computing Systems, ACM Journal of Emerging Technologies, and Journal of Low Power Electronics; served as guest editor of IEEE Design & Test of Computers (2010, 2013) and IEEE Journal on Emerging and Selected Topics in Circuits and Systems (2014). He has served as co-program chair of IEEE IMS3TW 2011, IEEE NANOARCH 2013, IEEE VDAT 2014, and IEEE HOST 2015, and in the program committee of several IEEE/ACM conferences. Dr. Bhunia received his PhD from Purdue University on energy-efficient and robust electronics. He is a senior member of IEEE.

Plenary Talk 5

3:30pm ~ 4:00pm, Tuesday July 10, 2018

Designing Safety-critical Systems: Rapidly and Accurately!

Ulf Schlichtmann
Professor, Electrical and Computer Engineering
Technical University of Munich

Summary
Thanks to still ever increasing advances in manufacturing technology, we can implement ever more complex systems. System-level design is essential to deal with the enourmous complexity of today's advanced systems. At the same time, fast time to market is as essential as ever. And robustness and reliability are increasing in importance, as the focus of the semiconductor industry shifts to applications with high safety requirements such as automotive. High-level system models, known as Virtual Prototypes, are essential to meet all these challenges. Fault injection is the most common technique to evaluate system robustness.

I will outline some recent progress in Virtual Prototypes for safety evaluations. I will especially discuss how both high performance and high accuracy in fault injection can be achieved at the same time. Robustness evaluation has to be extended to Firmware in addition to Hardware. Future challenges for system design will conclude my presentation.

About Ulf Schlichtmann
Ulf Schlichtmann holds a Dipl.-Ing. degree (MSc equivalent) and a doctorate in electrical engineering from TUM, as well as a technology business degree. He spent about 10 years in the semiconductor industry (Siemens, Infineon) in various engineering, management and executive positions, working on design automation, design libraries, IP reuse, and product development.

In 2003, he joined TUM as professor and head of the Chair of Electronic Design Automation. From 2007-2013 he served as Dean and Vice Dean of TUM's Department of Electrical and Computer Engineering (ECE). Since 2016, Ulf is an elected member of TUM's Academic Senate as well as the TUM Board of Trustees. Since 2017, he is a member of the Advisory Council of TUM's Institute for Advanced Studies. Also, since 2017, Ulf serves as Vice Dean of TUM's ECE Department again. Ulf is currently a visiting Professor at Nanyang Technological University (NTU), Singapore as well as Honorary Chair Professor at National Taiwan University of Science and Technology (NTUST), Taipei.

Ulf's current research interests include computer-aided design of electronic circuits and systems, with an emphasis on designing reliable and robust systems. His research increasingly focuses on emerging technologies, such as microfluidic biochips and photonic interconnects.

ISVLSI 2018 Program

Note: Best paper candidates are denoted with "" ahead of their titles.*

Monday, July 9 2018

Session 01

Analog and Mixed Signal I

Chair: ***Pallab Dasgupta, India IIT Kharagpur***
Room: ***N001***

9:50 AM
Gyrator-C based Bandpass Filter with Improved Dynamic Range for Fully Integrated RF Front-end
Lakshmi N S and Bhaskar M

10:10 AM
Replica-Based Low Drop-Out Voltage Regulator with Assistant Power Transistors for Digital VLSI Systems
Yang Nan, Chenchang Zhan, Guanhua Wang, Linjun He and Han Li

10:30 AM
Area Efficient NMOS based Positive and Negative Voltage Multiplier
Vikas Rana

Session 02

Digital Circuits and FPGA based Design I

Chair: ***Mingjie Lin, University of Central Florida***
Room: ***N002***

9:50 AM
Achieving Low Power Classification with Classifier Ensemble
Fanglei Hu, Min Zhang and Hailong Jiao

10:10 AM
A Power-efficient Hybrid Architecture Design for Image Recognition using CNNs
Jinhang Choi, Srivatsa Srinivasa, Yasuki Tanabe, Jack Sampson and Vijaykrishnan Narayanan

10:30 AM
Towards Budget-Driven Hardware Optimization for Deep Convolutional Neural Networks using Stochastic Computing
Zhe Li, Ji Li, Ao Ren, Caiwen Ding, Jeffrey Draper, Qinru Qiu, Bo Yuan and Yanzhi Wang

Session 03

Testing, Reliability, and Fault-Tolerance I

Chair: ***Rung-Bin Lin, Yuan Ze University***
Room: ***N003***

9:50 AM
Fast Heuristics for Near Optimal Signal Restoration in Post-Silicon Validation
Xiaobang Liu and Ranga Vemuri

10:10 AM
PGIREM: Reliability-Constrained IR Drop Minimization and Electromigration Assessment of VLSI Power Grid Networks using Cooperative Coevolution
Sukanta Dey, Satyabrata Dash, Sukumar Nandi and Gaurav Trivedi

10:30 AM
Silicon Debug with Maximally Expanded Internal Observability using Nearest Neighbor Algorithm
Ankit Jindal, Binod Kumar, Nitish Jindal, Masahiro Fujita and Virendra Singh

Session 04

Computer Aided Design and Verification I

Chair: ***YongFu Li, Global Foundries***
Room: ***N001***

10:50 AM
Application Specific Networks-on-Chip Synthesis: An Energy Efficient Approach
Somayeh Kashi, Ahmad Patooghy, Dara Rahmati, Mahdi Fazeli and Michel Kinsy

11:10 AM
Accurate Models for Optimizing Tapered Microchannel Heat Sinks in 3D ICs
Leslie Hwang, Beomjin Kwon and Martin Wong

11:30 AM
Designing and Benchmarking of Double-Row Height Standard Cells
Yu-Xiang Chiang, Cheng-Wei Tai, Shang-Rong Fang, Kai-Chun Peng, Yuan-Dar Chung, Jin-Kai Yang and Rung-Bin Lin

Session 05

Emerging and Post-CMOS Technologies I

Chair: ***Kang Wang, Beihang University***
Room: ***N002***

10:50 AM
Dual-Threshold Directed Execution Progress Maximization for Nonvolatile Processors
Dongqin Zhou, Keni Qiu, Yuanchao Xu, Xin Shi and Yongpan Liu

11:10 AM
***A Comprehensive Electro-Optical Model for Silicon Photonic Switches**
Xuanqi Chen, Zhifei Wang, Yi-Shing Chang, Jiang Xu, Peng Yang, Zhehui Wang and Luan H.K. Duong

11:30 AM
CMOS Gates with Second Function
Jan Nevoral, Richard Ruzicka and Vaclav Simek

Session 06

System Design and Security I

Chair: ***Xiaochen Guo, Lehigh University***
Room: ***N003***

10:50 AM
Tagless DRAM Cache
S R Swamy Saranam Chongala and Madhu Mutyam

11:10 AM
CT-Cache: Compressed Tag-Driven Cache Architecture
Haeyoon Cho, Joonho Kong, Arslan Munir and Naresh Kumar Giri

11:30 AM
High Bandwidth Off-Chip Memory Access through Hybrid Switching and Inter-Chip Wireless Links
Sri Harsha Gade, Hemanta Kumar Mondal and Sujay Deb

SPECIAL Session 01

Shall We Jointly Address VLSI Reliability and Security?

Chair: ***Qiaoyan Yu, University of New Hampshire, USA;***
Michel A. Kinsy, Boston University, USA
Room: ***N001***

3:50 PM
Investigating Reliability and Security of Integrated Circuits and Systems
Qiaoyan Yu, Zhiming Zhang, and Jaya Dofe

4:10 PM
Reliability and Security in Non-volatile Processors, Two Sides of the Same Coin
Patrick Cronin, Chengmo Yang, and Yongpan Liu

4:30 PM
A Short Survey at the Intersection of Reliability and Security in Processor Architecture Designs
Lake Bu, Miguel Mark, and Michel Kinsy

4:50 PM
Can Soft Errors Be Handled Securely?
Senwen Kan, Jennifer Dworak

Session 07

System Design and Security II

Chair: ***Zhongfeng Wang, Nanjing University***
Room: ***N002***

3:50 PM
***BD-NET: A Multiplication-less DNN with Binarized Depthwise Separable Convolution**
Zhezhi He, Shaahin Angizi, Adnan Siraj Rakin and Deliang Fan

4:10 PM
TaiJiNet: Towards Partial Binarized Convolutional Neural Network for Embedded Systems
Yingjian Ling, Kan Zhong, Yunsong Wu, Duo Liu, Jinting Ren, Renping Liu, Moming Duan, Weichen Liu and Liang Liang

4:30 PM
An ECC-Free MLC STT-RAM based Approximate Memory Design for Multimedia Applications
Zihao Liu, Tao Liu, Jie Guo, Nansong Wu and Wujie Wen

4:50 PM
Robust Timing Attack Countermeasure on Virtual Hardware
Kai Yang, Jungmin Park, Mark Tehranipoor and Swarup Bhunia

SPECIAL Session 02

Emerging Computing and Memory Technologies at Post-CMOS Era

Chair: ***Liang Shi, Chongqing University; Bei Yu, The Chinese University of Hong Kong***
Room: ***N003***

3:50 PM
Towards Theoretical Cost Limit of Stochastic Number Generators for Stochastic Computing
Meng Yang, Bingzhe Li, David J. Lilja, Bo Yuan, Weikang Qian

4:10 PM
An Energy-Efficient PIM-Accelerator Simulation Framework
Di Gao, Tianhao Shen, Cheng Zhuo

4:30 PM
Efficient Self-balancing Binary Search Tree for Non-Volatile Memory with Write Asymmetry
Ming-Chang Yang

4:50 PM
Minimizing the Energy Consumption of MLC STT-RAM Main Memory with Asymmetric Write Energy by Re-designing Cache Management
Tseng-Yi Chen

Poster Session

5:30pm ~ 7:10pm
Room: ***N103***

P1.
Fully-on-Chip Digitally Assisted LDO Regulator with Improved Regulation and Transient Responses
Han Li, Chenchang Zhan and Ning Zhang

P2.
A Novel Asynchronous Analog to Digital Converter for Surveillance Camera Applications
Siddharth Kala, Sunil R., Nithin Kumar Y.B., Vasantha M.H. and Edoardo Bonizzoni

P3.
An Integrated MaxFit Genetic Algorithm-SPICE Framework for 2-stage Op-amp Design Automation
Harsha M. V. and B. P. Harish

P4.
Mismatch Resilient 3.5-bit MDAC with MCS-CFCS
Satyajit Mohapatra, Hari Gupta and Nihar Mohapatra

P5.
Design of Low Power SAR ADC using Clock Retiming
Jalaja S and Vijaya Prakash A M

P6.
A 375 nA Input Off Current Schmitt Triger LDO for Energy Harvesting IoT Sensors
Koichiro Ishibashi and Shiho Takahashi

P7.
Precise Duty Cycle Variation Detection and Self-Calibration System for High-Speed Data Links
Karen Khachikyan, Abraham Balabanyan and Hrachya Gumroyan

P8.
Parametric Circuit Optimization with Reinforcement Learning
Changcheng Tang, Zuochang Ye and Yan Wang

P9.
End-to-End Industrial Study of Retiming
Cunxi Yu, Chau-Chin Huang, Gi-Joon Nam, Mihir Choudhury, Victor N. Kravets, Andrew Sullivan, Maciej Ciesielski and Giovanni De Micheli

P10.
Communication-aware Module Placement for Lowering Power in Large FPGA Designs
Kalindu Herath, Alok Prakash, Udaree Kanewala and Thambipillai Srikanthan

P11.
A Novel Mixed-Size Fixed-Ouline Floorplacement Algorithm
Qian Chen and Sheqin Dong

P12.
ARCHVerifyr: An Embedded Software-Driven Approach for Architecture Verification
Tomas Grimm, Djones Lettnin and Michael Huebner

P13.
High-average and Guaranteed Performance for Wireless Networks-on-Chip Architectures
Mohammad Baharloo, Ahmad Khonsari, Pouya Shiri, Iman Namdari and Dara Rahmati

P14.
Hardware Implementation of Reconfigurable Separable Convolution
Lei Rao, Bin Zhang and Jizhong Zhao

P15.
Low Overhead Online Checkpoint for Intermittently Powered Non-volatile FPGAs
Xinyi Zhang, Clay Patterson, Yongpan Liu, Chengmo Yang, Chun Jason Xue and Jingtong Hu

P16.
Pixel-Parallel Architecture for Neuromorphic Smart Image Sensor with Visual Attention
Md Jubaer Hossain Pantho, Pankaj Bhowmik and Christophe Bobda

P17.
Lightweight ASIC Implementation of AEGIS-128
Anubhab Baksi, Vikramkumar Pudi, Swagata Mandal and Anupam Chattopadhyay

P18.
Architecture Exploration and Delay Minimization Synthesis for SET-Based Programmable Gate Arrays
Chia-Cheng Wu, Kung-Han Ho, Juinn-Dar Huang and Chun-Yao Wang

P19.
MRAM-on-FDSOI Integration: A Bit-cell Perspective
Hao Cai, You Wang, Wang Kang, Lirida Naviner, Xinning Liu, Jun Yang and Weisheng Zhao

P20.
High Performance Ternary Multiplier using CNTFET
Subhendu Kumar Sahoo, Krishna Dhoot, and Rasmita Sahoo

P21.

A Robust Dual Reference Computing-in-Memory Implementation and Design Space Exploration Within STT-MRAM

Liuyang Zhang, Wang Kang, Hao Cai, Peng Ouyang, Lionel Torres, Youguang Zhang, Aida Todri-Sanial and Weisheng Zhao

P22.

Biosensing Performance Optimization of DMFET for Fully Filled and Partially Filled Cavity

Ankita Porwal and Chitrakant Sahu

P23.

A Dynamic Resource Allocation Strategy for NoC Based Multicore Systems with Permanent Faults

Suraj Paul, Navonil Chatterjee and Prasun Ghosal

P24.

Floorplanning in Graphene Nanoribbon (GNR) Based Circuits

Subrata Das and Debesh Das

P25.

Generating Safety Guidance for Medical Injection with Three-Compartment Pharmacokinetics Model

Cunxi Yu, Heinz Riener, Francesca Stradolini and Giovanni De Micheli

P26.

A Novel Approach for Nearest Neighbor Realization of 2D Quantum Circuits

Anirban Bhattacharjee, Chandan Bandyopadhyay, Robert Wille, Rolf Drechsler and Hafizur Rahaman

P27.

A Hardware-efficient Implementation of CLOC for On-Chip Authenticated Encryption

Mahmoud A. Elmohr, Sachin Kumar, Mustafa Khairallah and Anupam Chattopadhyay

P28.

0.9 to 2.5 GHz Sub-sampling Receiver Architecture for Dynamically Reconfigurable SDR

Ajinkya Kale, Johannes Sturm and Vijaya Sankara Rao Pasupureddi

P29.

Hardware Obfuscation using Strong PUFs

Soroush Khaleghi and Wenjing Rao

P30.

Multi-Block APUF with 2-level Voltage Supply

Yunxi Guo, Timothy Dee and Akhilesh Tyagi

P31.

Write energy optimization for STT-MRAM cache with data pattern characterization

Bi Wu, Xiaolong Zhang, Yuanqing Cheng, Zhaohao Wang, Dijun Liu, Youguang Zhang and Weisheng Zhao

P32.

Time Stamp Based Scheduling for Energy Harvesting Systems with Hybrid Nonvolatile Hardware Support

Xin Shi, Tongda Wu, Keni Qiu, Huazhong Yang and Yongpan Liu

P33.

EETD: An Energy Efficient Design for Runtime Hardware Trojan Detection in Untrusted Network-on-Chip

Mubashir Hussain, Amin Malekpour, Hui Guo and Sri Parameswaran

P34.

Combining Symbolic Computer Algebra and Boolean Satisfiability for Automatic Debugging and Fixing of Complex Multipliers

Alireza Mahzoon, Daniel Grosse and Rolf Drechsler

P35.
Enhancing lifetime of PCM-based main memory with Efficient Recovery of Stuck-at Faults
Marjan Asadinia and Christophe Bobda

Student Research Forum

5:30pm ~ 7:10pm
Room: ***N103***
Cadence Introduction from 5:30pm to 5:45pm

F1.
Guessing your PIN right: Unlocking smartphones with publicly available sensor data
David Berend, Bernhard Jungk and Shivam Bhasin

F2.
Synthesis, Technology Mapping and for Emerging Technologies
Debjyoti Bhattacharjee and Anupam Chattopadhyay

F3.
Logic Synthesis for In-Memory Computing using Resistive Memories
Saeideh Shirinzadeh and Rolf Drechsler

F4.
Minimalistic Perspective to Public Key Implementations on FPGA
Debapriya Basu Roy and Debdeep Mukhopadhyay

F5.
Development of High-Stability, Low-Leakage 6Tr-SRAM with Single Data Line and Single Power Supply Using SOTB Process
Shin Miyamoto and Nobuaki Kobayashi

F6.
Exploiting Principle of Moving Target Defense to Secure FPGA Systems
Zhiming Zhang and Qiaoyan Yu

Tuesday, July 10 2018

Session 08

System Design and Security III

Chair: ***Theocharis Theocharides, University of Cyprus***
Room: ***N001***

9:50 AM
A Highly Flexible Lightweight and High Speed True Random Number Generator on FPGA
Faqiang Mei, Lei Zhang, Chongyan Gu, Yuan Cao, Chenghua Wang and Weiqiang Liu

10:10 AM
LUT-Lock: A Novel LUT-based Logic Obfuscation for FPGA-Bitstream and ASIC-Hardware Protection
Hadi Mardani Kamali, Kimia Zamiri Azar, Kris Gaj, Houman Homayoun and Avesta Sasan

10:30 AM
ArtiFact: Architecture and CAD Flow for Efficient Formal Verification of SoC Security Policies
Atul Prasad Deb Nath, Swarup Bhunia and Sandip Ray

Session 09

Computer Aided Design and Verification II

Chair: ***Wei-Kei Mark, National Tsinghua University***
Room: ***N002***

9:50 AM
***Identifying Lithography Weak-points of Standard Cells with Partial Pattern Matching**
Yongfu Li, I-Lun Tseng, Zhao Chuan Lee, Valerio Perez, Vikas Tripathi and Jonathan Yoong Seang Ong

10:10 AM
Feature Based Coverage Analysis of AMS Circuits
Antara Ain, Akshay Mambakam and Pallab Dasgupta

10:30 AM
SAT Encoding-based Verification of Sneak Path Problem in Via-switch FPGA
Ryutaro Doi and Masanori Hashimoto

Session 10

Emerging and Post-CMOS Technologies II

Chair: ***Prasun Ghosal, Indian Institute of Engineering Science and Technology, Shibpur***
Room: ***N003***

9:50 AM
RRAM Based Buffer Design for Energy Efficient CNN Accelerator
Kaiyuan Guo, Jincheng Yu, Xuefei Ning, Yiming Hu, Yu Wang and Huazhong Yang

10:10 AM
A Mixed-Mode Neuron with On-Chip Tunability for Generic Use in Memristive Neuromorphic Systems
Sagarvarma Sayyaparaju, Ryan Weiss and Garrett S. Rose

10:30 AM
Harnessing Emerging Technology for Compute-In-Memory Support
Nicholas Jao, Akshay Krishna Ramanathan, Srivatsa Srinivasa, Sumitha George, John Sampson, and Vijaykrishnan Narayanan

Session 11

Analog and Mixed Signal II

Chair: ***Saraju Mohanty, University of North Texas***
Room: ***N001***

10:50 AM
91 dB Dynamic Range 9.5 nW Low Pass Filter for Bio-Medical Applications
Jayaram Reddy M K, Sreenivasulu Polineni and Laxminidhi Tonse

11:10 AM
***A Low Power, High Gain Semi-Floating Gate Amplifier for Resonating Sensors Front-End**
Luca Marchetti, Yngvar Berg and Mehdi Azadmehr

11:30 AM
A High-Efficient Current-Mode PWM DC-DC Buck Converter Using Dynamic Frequency Scaling
Ankit Rehani, Sujay Deb, Pydi Ganga Bahubalindruni, Bhavin Odedara and Srikanth Bojja

Session 12

System Design and Security IV

Chair: ***Deliang Fan, University of Central Florida***
Room: ***N002***

10:50 AM
An Adversarial Example Restoration System for Neuromorphic Computing Security
Chenchen Liu, Qide Dong, Fuxun Yu and Xiang Chen

11:10 AM
MAT: A Multi-strength Adversarial Training Method to Mitigate Adversarial Attacks
Chang Song, Hsin-Pai Cheng, Huanrui Yang, Sicheng Li, Chunpeng Wu, Qing Wu, Yiran Chen and Hai Li

11:30 AM
Hu-Fu: Hardware and Software Collaborative Attack Framework against Neural Networks
Wenshuo Li, Jincheng Yu, Xuefei Ning, Pengjun Wang, Qi Wei, Yu Wang and Huazhong Yang

Tutorial

Memristive Devices for Computing: Circuits, Architectures and Applications

10:50am ~ 11:50am
Room: ***N003***

Speaker: ***Said Hamdioui, Delft University of Technology***

Both today's computer architectures and device technologies (used to manufacture them) are facing major challenges making them incapable to deliver the required functionalities and features. Computers are facing the three well-known walls, which are the memory wall, the instruction level parallelism wall, and the power wall. Meanwhile, nanoscale CMOS technology also faces three walls, which are the reliability wall, the leakage wall, and the cost wall. All of these have led to the slowdown of the traditional device scaling. Thus, alternative computing architectures and notions have to be explored in the light of emerging new device technologies. In this session/tutorial, we will explore the potential of memristor devices (as emerging devices) for enabling a new computing paradigm, called "computation-in-memory" (as an alternative architecture), covering the topics of the memory, logic design, and computing with memristive devices.

SPECIAL Session 03

Essential Keys to Manufacturability: Layout Features and Lithography Technologies

Chair: ***Wai-Kei Mak, National Tsing Hua University; Cheng Zhuo, Zhejiang University***
Room: ***N001***

4:20 PM
Sparse VLSI Layout Feature Extraction: A Dictionary Learning Approach
Hao Geng, Haoyu Yang, Bei Yu, Xingquan Li, Xuan Zeng

4:40 PM
Pattern Similarity Metrics for Layout Pattern Classification and their Validity Analysis by Lithographic Responses
Atsushi Takahashi, Shimpei Sato, Hiroki Ogura, Yu-Min Sung, Ting-Chi Wang

5:00 PM
Recent research and challenges in multiple patterning layout decomposition
Iris Hui-Ru Jiang, Hua-Yu Chang

5:20 PM
Guiding Template-induced Design Challenges in DSA-MP Lithography
Shao-Yun Fang, Kuo-Hao Wu

Session 13

Digital Circuits and FPGA based Designs II

Chair: ***Weikang Qian, Shanghai Jiaotong University***
Room: ***N002***

4:20 PM
***FPAP: A Folded Architecture for Efficient Computing of Convolutional Neural Networks**
Yizhi Wang, Jun Lin and Zhongfeng Wang

4:40 PM
Hyperdrive: A Systolically Scalable Binary-Weight CNN Inference Engine for mW IoT End-Nodes
Renzo Andri, Lukas Cavigelli, Davide Rossi and Luca Benini

5:00 PM
An Optimized Architecture For Decomposed Convolutional Neural Networks
Fangxuan Sun, Jun Lin and Zhongfeng Wang

5:20 PM
Interconnect Delay Analysis for RRAM Crossbar based FPGA
Masanori Hashimoto, Yuki Nakazawa, Ryutaro Doi, Jaehoon Yu

SPECIAL Session 04

Emerging Trends in Energy Efficient and Secure Neural Network Acceleration

Chair: ***Deliang Fan, University of Central Florida; Yanzhi Wang, Northeastern University***
Room: ***N003***

4:20 PM
Security challenges in smart surveillance systems and new design opportunities
Hai Li

4:40 PM
Enhancing the Robustness of Deep Neural Networks from ``Smart" Compression
Tao Liu, Zihao Liu, Qi Liu, Wujie Wen

5:00 PM
Accelerating Low Bit-Width Deep Convolution Neural Network in MRAM
Zhezhi He, Shaahin Angizi, Deliang Fan

5:20 PM
Emerging Neuromorphic Computing Paradigms Exploring Magnetic Skyrmions
Sai Li, Wang Kang, Xing Chen, Jinyu Bai, Biao Pan, Youguang Zhang and Weisheng Zhao

Session 14

System Design and Security V

Chair: ***Keni Qiu, Capital Normal University***
Room: ***N001***

9:50 AM
Security-Driven Task Scheduling for Multiprocessor System-on-Chips with Performance Constraints
Nan Wang, Manting Yao, Dongxu Jiang, Song Chen, Yu Zhu

10:10 AM
A Hardware Monitor to Protect Linux System Calls
George Provelengios, Arman Pouraghily, Russell Tessier and Tilman Wolf

10:30 AM
Towards Dynamic Execution Environment for System Security Protection against Hardware Flaws
Kenneth Schmitz, Oliver Keszocze, Jurij Schmidt, Daniel Grosse and Rolf Drechsler

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Wednesday, July 11 2018

Session 15

Digital Circuits and FPGA Based Designs III

Chair: ***Chenchen Liu, Clarkson University***
Room: ***N002***

9:50 AM
A Fast and Effective Memristor-Based Method for Finding Approximate Eigenvalues and Eigenvectors of Non-Negative Matrices
Chenghong Wang, Zeinab S. Jalali, Caiwen Ding, Yanzhi Wang and Sucheta Soundarajan

10:10 AM
A Low-Power and Small-Area Multiplier for Accuracy-Scalable Approximate Computing
Hiroyuki Baba, Tongxin Yang, Masahiro Inoue, Kaori Tajima, Tomoaki Ukezono and Toshinori Sato

10:30 AM
A Hardware/Software Co-Design Method for Approximate Semi-supervised K-Means Clustering
Pengfei Huang, Chenghua Wang, Ruizhe Ma, Weiqiang Liu and Fabrizio Lombardi

SPECIAL Session 05

Intelligent Methods & Techniques for Reliable and Adaptive Multicore/Manycore System

Chair: ***Theocharis (Theo) Theocharides, University of Cyprus;***
Prasun Ghosal, IIEST, Shibpur, India
Room: ***N003***

9:50 AM
Robustness for Smart Cyber Physical Systems and Internet-of-Things: From Adaptive to Intelligent Methods for Reliability and Security
Florian Kriebel, Semeen Rehman, Muhammad Abdullah Hanif, Faiq Khalid, Muhammad Shafique

10:10 AM
On how to efficiently implement Deep Learning algorithms on PYNQ platform
Luca Stornaiuolo, Marco D. Santambrogio, Donatella Sciuto

10:30 AM
Enabling Reliable High Throughput On-Chip Wireless Communication for Many Core Architectures
Sri Harsha Gade, Mitali Sinha, Sidhartha Sankar Rout, Sujay Deb

Session 16

Testing, Reliability, and Fault-Tolerance II

Chair: ***Hailong Yao, Tsinghua University***
Room: ***N001***

10:50 AM
Predicting the tolerance of Extreme Electromagnetic Interference on MOSFETs
Nishchay Sule, Troy Powell, Sameer Hemmady and Payman Zarkesh-Ha

11:10 AM
Enhancing Observability for Post-Silicon Debug with On-Chip Communication Monitors
Yuting Cao, Hernan Palombo, Sandip Ray and Hao Zheng

11:30 AM
Performance Enhancement of Split Length Compensated Operational Amplifiers
Donel Anto, Abhijeet D. Taralkar, Nithin Kumar Y. B. and Vasantha M. H.

Session 17

System Design and Security VI

Chair: ***Mike Borowczak, University of Wyoming***
Room: ***N002***

10:50 AM
Design-Based Fingerprinting Using Side-Channel Power Analysis For Protection Against IC Piracy
James Shey, Naghmeh Karimi, Ryan Robucci and Chintan Patel

11:10 AM
PPAP and iPPAP: PLL based Protection Against Physical attacks
Prasanna Ravi, Shivam Bhasin, Jakub Breier and Anupam Chattopadhyay

11:30 AM
Mystic: Mystifying IP Cores Using an Always-ON FSM Obfuscation Method
Ahmad Patooghy, Ehsan Aerabi, Hamidreza Rezaei, Miguel Mark, Mahdi Fazeli, and Michel A. Kinsy

Session 18

Digital Circuits and FPGA Based Designs IV

Chair: ***Ming-Chang Yang, Chinese University of Hong Kong***
Room: ***N003***

10:50 AM
FPGA-based Controllers for Compact Low Power Refreshable Braille Display
Suman Muralikrishnan, Pulkit Sapra, Saurabh Agrawal, Piyush Chanana, M. Balakrishnan and P.V.M. Rao

11:10 AM
Very Large-Scale and Node-Heavy Graph Analytics with Heterogeneous FPGA+CPU Computing Platform
Yu Zou and Mingjie Lin

11:30 AM
On-chip Data Security against Untrustworthy Software and Hardware IPs in SoC FPGAs
Sreecharan Gundabolu and Xiaofang Wang

SPECIAL Session 06

Microfluidic Large Scale Integration (mVLSI): Recent Developments and Upcoming Challenges

Chair: ***Bing Li, Technical University of Munich; Hao Yu, Southern University of Science and Technology***
Room: ***N001***

2:30 PM
Design Automation and Test for Flow-Based Biochips: Past Successes and Future Challenges
Tsung-Yi Ho

2:50 PM
Multi-Target Many-Reactant Sample Preparation for Reactant Minimization on Microfluidic Biochips
Yung-Chun Lei, Tien-Kuo Lin, Juinn-Dar Huang

3:10 PM
More Effective Randomly-Designed Microfluidics
Weiqing Ji, Tsung-Yi Ho, Hailong Yao

3:30 PM
Accelerating Simulation of Particle Trajectories in Microfluidic Devices by Constructing a Cloud Database
Junchao Wang, Lingxuan Fu, Liyang Yu, Xiwei Huang, Philip Brisk, William H. Grover

SPECIAL Session 07

Secure Hardware Design for Distributed Agents

Chair: ***Mike Borowczak, University of Wyoming; Saraju Mohanty, University of North Texas***
Room: ***N002***

2:30 PM
PUF-based Secure Test Wrapper for SoC Testing
Sudeendra Kumar, Saurabh Seth, Sauvagya Sahoo, Abhishek Mahapatra, Ayas Kanta Swain, and Kamalakanta Mahapatra

2:50 PM
Detection of Sequential Trojans in Embedded System Designs without Scan Chains
Pranav Dharmadhikari, Akhilesh Raju, Ranga Vemuri

3:10 PM
Designing for Security Within and Between IoT Devices
Mike Borowczak, Rafer Cooley, and Shaya Wolf

3:30 PM
A Two-Tiered Heterogeneous and Reconfigurable Application Processor for Future Internet of Things
Prasanna Kansakar, Arslan Munir

SPECIAL Session 08

Embedded Multi-Core in Automotive and I4.0

Chair: ***Ming-Chang Yang, Chinese University of Hong Kong***
Room: ***N003***

2:30 PM
Glimpse of Domain Control Unit Software Architecture for Intelligent Connected Vehicle
Sun Hua, United Automotive Electronic Systems Co., Ltd

2:50 PM
The challenges of E/E architecture design for EV
Sam QIN, Intron / G-Pulse

3:10 PM
Heterogenous HPC Multi-Core Platforms and Tools - Functional Intelligence and Digital Integration in Cyber-Physical Systems (CPS)
Juergen Becker, Karlsruhe Institute of Technology

SPECIAL Session 09

Energy Efficient and Hardware Secured Architectures for Smart Electronics I

Chair: ***Saraju P. Mohanty, University of North Texas, USA;***
Hui Zhao, University of North Texas, USA
Room: ***N001***

4:10 PM
Solar Cell Based Physically Unclonable Function for Cybersecurity in IoT Devices
S. Dinesh Kumar, Carson Labrado, Riasad Badhan, Himanshu Thapliyal, Vijay Singh

4:30 PM
Designing Scalable Hybrid Wireless NoC for GPGPUs
Hui Zhao, Xianwei Cheng, Saraju P. Mohanty, Juan Fang

4:50 PM
Functional Obfuscation of DSP cores using Robust Logic Locking and Encryption
Anirban Sengupta, Saraju P. Mohanty

SPECIAL Session 10

Timing in the Nanometer Era

Chair: ***Masanori Hashimoto, Osaka University; Bing Li, Technical University of Munich***
Room: ***N002***

4:10 PM
Distributed Timing Analysis at Scale
Martin D. F. Wong, Tsung-Wei Huang

4:30 PM
Timing Macro Modeling for Efficient Hierarchical Timing Analysis
Iris Hui-Ru Jiang, Pei-Yu Lee

4:50 PM
Timing with Virtual Signal Synchronization for Circuit Performance and Netlist Security
Grace Li Zhang, Bing Li, Ulf Schlichtmann

SPECIAL Session 11

Attacking Dynamic Optimizations in the Era of Complex Heterogeneous Multi-core Computing I

Chair: ***Jason Xue, City University of Hong Kong;***
Philip Brisk, University of California, Riverside
Room: ***N003***

4:10 PM
Realizing Closed-loop, Online Tuning and Control for Configurable-cache Embedded Systems: Progress and Challenges
Islam S. Badreldin, Ann Gordon-Ross, Tosiron Adegbija, Mohammad. H. Alsafrjalani

4:30 PM
An FPGA-based Brain Computer Interfacing using Compressive Sensing and Machine Learning
Ritu Ranjan Shrivastwa, Vikramkumar Pudi, Anupam Chattopadhyay

4:50 PM
Enabling efficient fine-grained DRAM activations with interleaved I/O
Chao Zhang, Xiaochen Guo

SPECIAL Session 12

Energy Efficient and Hardware Secured Architectures for Smart Electronics II

Chair: ***Saraju P. Mohanty, University of North Texas, USA;***
Hui Zhao, University of North Texas, USA
Room: ***N001***

5:10 PM
Obfuscation of Fault Secured DSP Design through Hybrid Transformation
Anirban Sengupta, Shubha Neema, Pallabi Sarkar, Sri Harsha P, Saraju P Mohanty, Mrinal Kanti Naskar

5:30 PM
Run Time Mitigation of Performance Degradation Hardware Trojan Attacks in Network on Chip
Manoj Kumar JYV, A. K. Swain, S. Kumar, S. R. Sahoo, K. K. Mahapatra

5:50 PM
Exploration on Routing Configuration of HNoC with Reasonable Energy Consumption
Juan Fang, Zeqing Chang, Yanjin Cheng, Hui Zhao

SPECIAL Session 13

Design Using Emerging Devices

Chair: ***Vijaykrishnan Narayanan, Penn State University; Xueqing Li, Tsinghua University***
Room: ***N002***

5:10 PM
Ferroelectric Transistors for Neuromorphic Computing
Asif Islam Khan

5:30 PM
Nonvolatile Memory and Computing Using Emerging Ferroelectric Transistors
Xueqing Li, Longqiang Lai

5:50 PM
Collective computing using phase transition based dynamical systems
Nikhil Shukla, Suman Datta, Arijit Raychowdhury

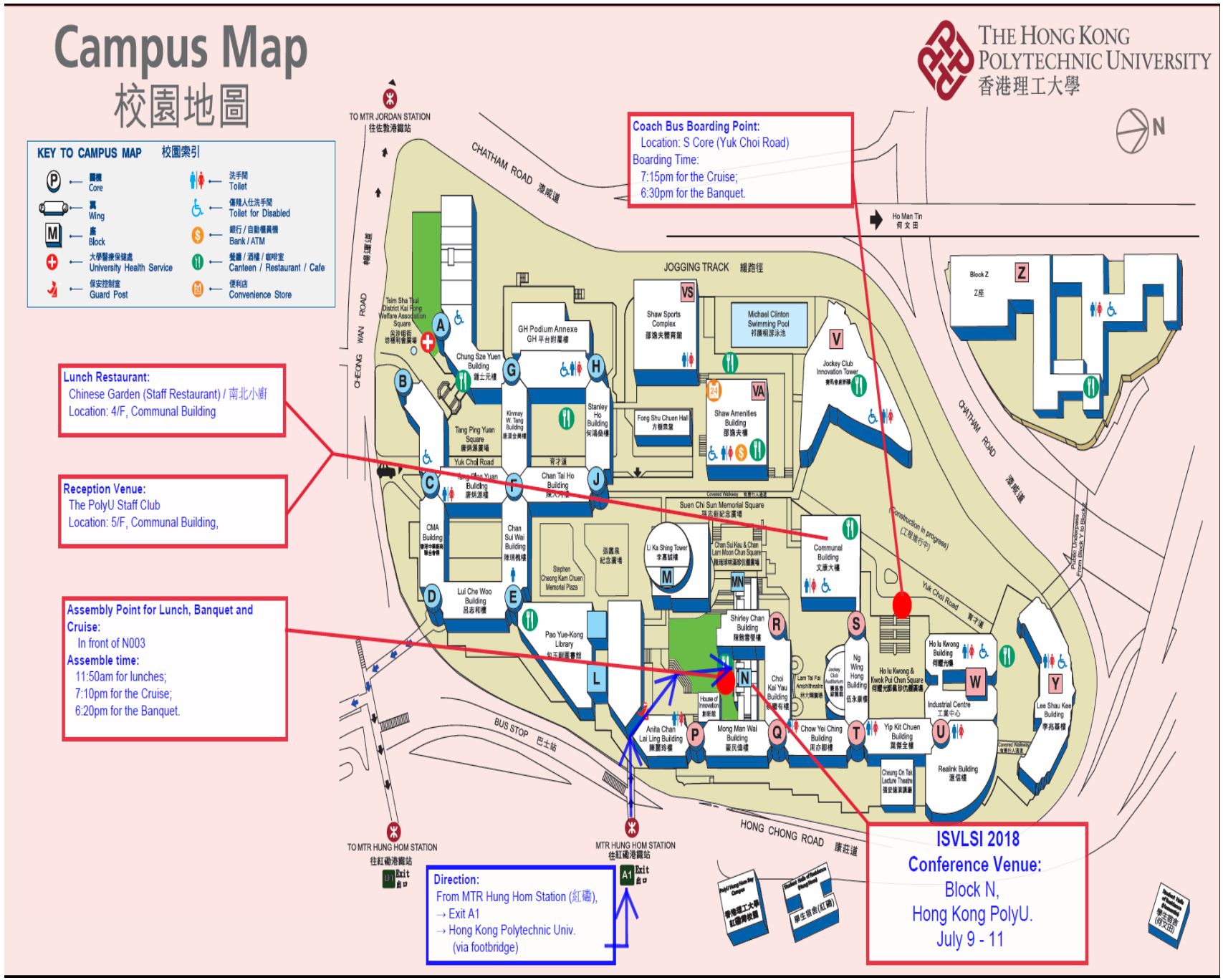
SPECIAL Session 14

Attacking Dynamic Optimizations in the Era of Complex Heterogeneous Multi-core Computing II

Chair: ***Jason Xue, City University of Hong Kong, Ann Gordon-Ross, University of Florida***
Room: ***N003***

5:10 PM
Software Support for Heterogeneous Computing
Siqi Wang, Alok Prakash, Tulika Mitra

5:30 PM
Predictive Modeling for CPU, GPU, and FPGA Performance and Power Consumption: A Survey
Kenneth O'Neal, Philip Brisk


Campus Map
校園地圖
THE HONG KONG POLYTECHNIC UNIVERSITY
香港理工大學
KEY TO CAMPUS MAP 校園索引
Core 核心
Wing 翼
Block 座
University Health Service 大學醫療保健處
Guard Post 保安控制室
Toilet 洗手間
Toilet for Disabled 傷殘人仕洗手間
Bank / ATM 銀行 / 自動櫃員機
Canteen / Restaurant / Cafe 餐廳 / 酒樓 / 咖啡室
Convenience Store 便利店
TO MTR JORDAN STATION 往佐敦港鐵站
CHATHAM ROAD 漆咸道
CHEONG WAN ROAD 長運道
JOGGING TRACK 緩跑徑
Coach Bus Boarding Point:
Location: S Core (Yuk Choi Road)
Boarding Time:
7:15pm for the Cruise;
6:30pm for the Banquet.
Ho Man Tin 何文田
Lunch Restaurant:
Chinese Garden (Staff Restaurant) / 南北小廚
Location: 4/F, Communal Building
Reception Venue:
The PolyU Staff Club
Location: 5/F, Communal Building,
Assembly Point for Lunch, Banquet and Cruise:
In front of N003
Assemble time:
11:50am for lunches;
7:10pm for the Cruise;
6:20pm for the Banquet.
Taim Sha Tsui District Kai Fong Welfare Association Square
Chung Sze Yuen Building 鍾士元樓
GH Podium Annexe GH 平台附屬樓
Shaw Sports Complex 邵逸夫體育館
Michael Clinton Swimming Pool 祁德頓游泳池
Jockey Club Innovation Tower
Block Z Z座
Kinmay W. Tang Building 鄧錦賢會堂
Stanley Ho Building 何鴻燊樓
Fong Shu Chuen Hall 方樹泉堂
Shaw Amenities Building 邵逸夫樓
Tang Ping Yuan Square 鄧炳源廣場
Yuk Choi Road 育才道
Yang Giles Yuan Building 楊葛洛源樓
Chan Tai Ho Building 陳大年樓
Suen Chi Sun Memorial Square 孫志新紀念廣場
CMA Building 會計及金融學院大樓
Chan Sui Wai Building 陳瑞機樓
Stephen Cheong Kam Chuan Memorial Plaza 張鑑泉紀念廣場
Li Ka Shing Tower 李嘉誠樓
Chan Sui Kau & Chan Lam Moon Chun Square 陳瑞球林蘭珍仿古廣場
Communal Building 文慶大樓
(Construction in progress) (工程進行中)
Lui Che Woo Building 呂志和樓
Pao Yue-Kong Library 包玉剛圖書館
Shirley Chan Building 陳啟宗樓
Ng Wing Hong Building 伍永康樓
Ho Iu Kwong Building 何耀光樓
Ho Iu Kwong & Kwok Pui Chun Square 何耀光郭鋇珍仿古廣場
Industrial Centre 工業中心
Lee Shau Kee Building 李兆基樓
House of Innovation 創新館
Anita Chan Lai Ling Building 陳麗玲樓
Mong Man Wai Building 蒙民偉樓
Choi Kai Yau Building 蔡繼有樓
Lam Tai Fai Amphitheatre 林大輝演奏廣場
Chow Yei Ching Building 周亦卿樓
Yip Kit Chuen Building 葉傑全樓
Realink Building 滙信樓
Cheung On Tak Lecture Theatre 張安達演講廳
Covered Walkway 有蓋行人通道
Podium Link Bridge From Block Z to Block Y
BUS STOP 巴士站
HONG CHONG ROAD 康莊道
TO MTR HUNG HOM STATION 往紅磡港鐵站
Exit D1 出口
MTR HUNG HOM STATION 往紅磡港鐵站
Exit A1 出口
Direction:
From MTR Hung Hom Station (紅磡),
→ Exit A1
→ Hong Kong Polytechnic Univ.
(via footbridge)
ISVLSI 2018
Conference Venue:
Block N,
Hong Kong PolyU.
July 9 - 11

Notes